

Compal Confidential

Schematics Document

Intel Chief River Platform

www.aitech1.ru

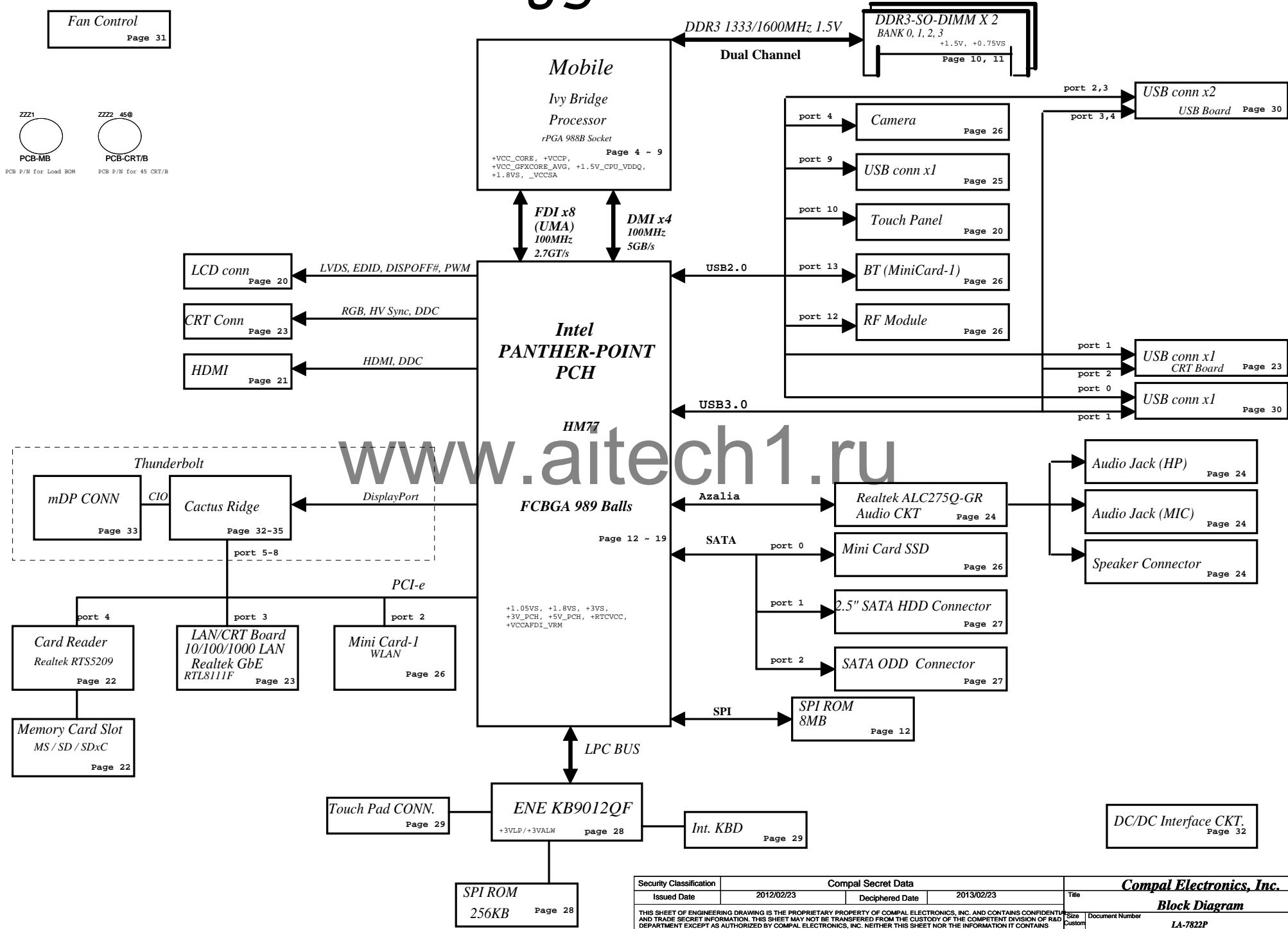
U5
LA-7822P

2012-02-23

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/02/23	Deciphered Date	2013/02/23	Title	Cover Sheet
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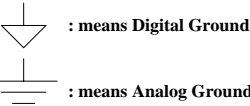
U5



Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VALW +3VALW	+3V_PCH +5V_PCH	+VCCP	+1.5V	+5VS +3VS +1.5VS +VCC_GFXCORE +VCCP +CPU_CORE +1.8VS +0.75VS +VCCSA +1.5V_CPU_VDDQ
S0	O	O	O	O	O	O	O
S3 / DC	O	O	O	O	X	O	X
S3 / AC	O	O	O	O	X	O	X
S3 / S4 / S5 WoLAN	O	O	O	O	X	X	X
S5 S4/AC	O	O	O	O	X	X	X
S5 S4/ Battery only	O	O	O	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X	X

Symbol Note :



PD@ : means Parade PS8710BT
PC@ : means PERICOM PI3EQX7502IZDEX
TB@ : means Thunderbolt
@ : means just reserve , no build
CONN@ : means ME part.

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

U5
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	26.1K +/- 5%	0.6191 V	0.683 V	0.7526 V
2	34.8K +/- 5%	0.7745 V	0.8519 V	0.9358 V
3	46.4K +/- 5%	0.9801 V	1.0459 V	1.1133 V
4	56.2K +/- 5%	1.1136 V	1.1873 V	1.2627 V
* 5	71.5K +/- 5%	1.2918 V	1.3758 V	1.4615 V
6	NC	2.500 V	3.300 V	3.300 V
7				

U5 ES0
U5 ES1
U5 ES2
U5 PP
U5 IRT

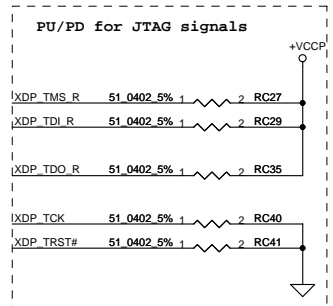
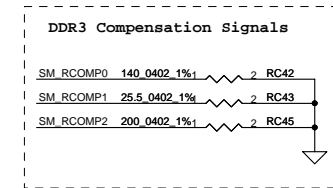
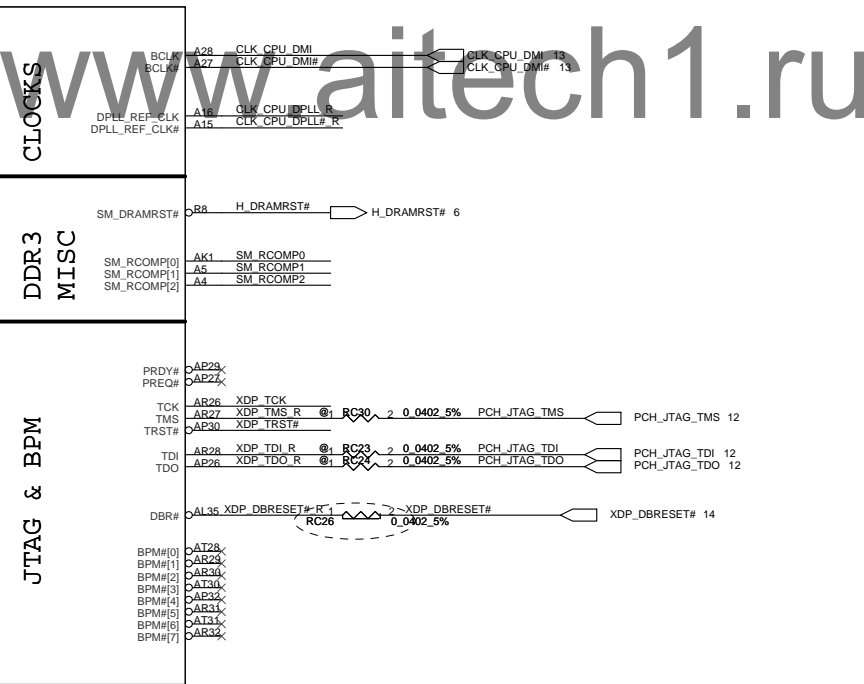
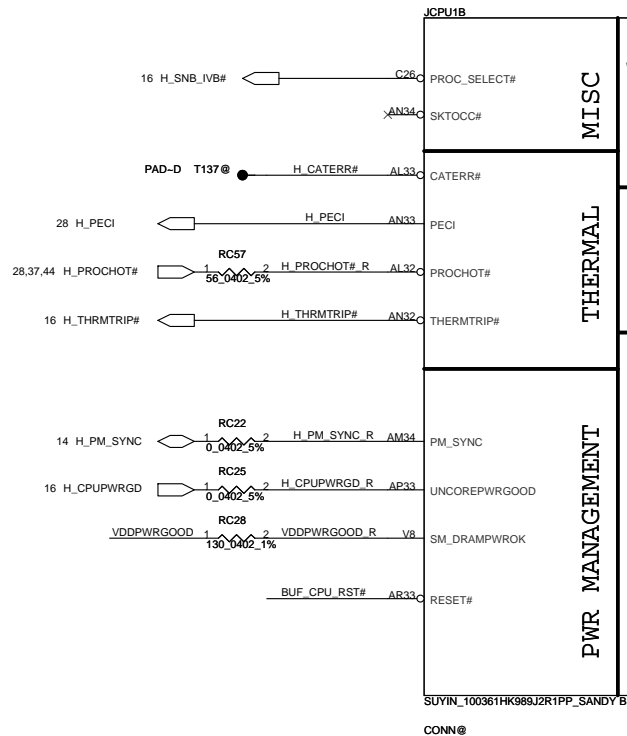
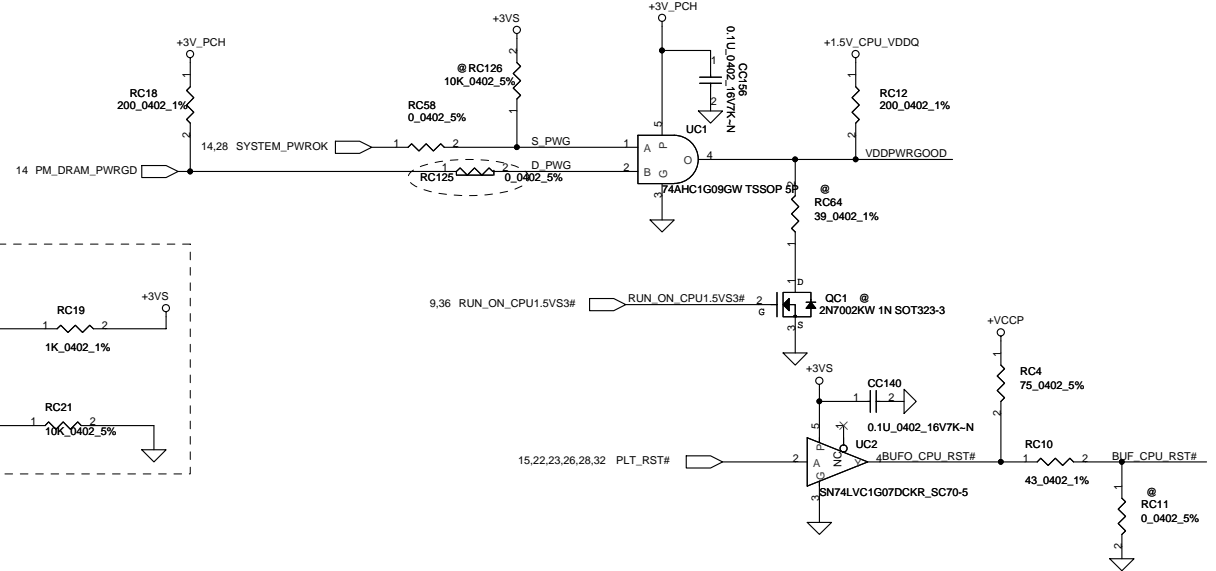
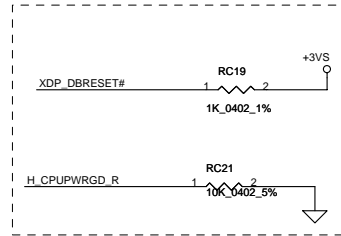
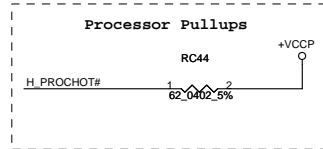
SMBUS Control Table

	SOURCE	BATT	XD	SODIMM	EC-KB930	Cactus Ridge	PCH	Smart Charge
SMB_EC_CK1 SMB_EC_DAI	EC	V	X	X	X	X	X	V
SMBCLK SMBDATA	PCH	X	V	V	X	X	X	X
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	V	X	X	X

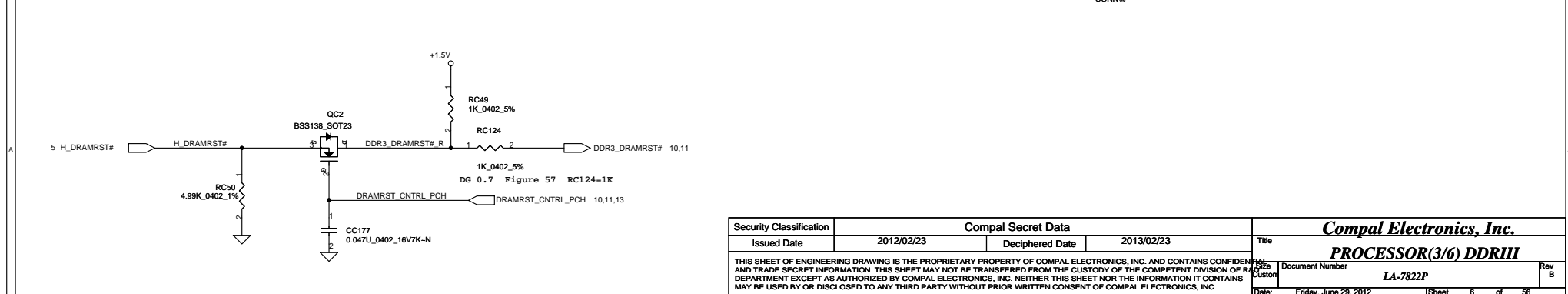
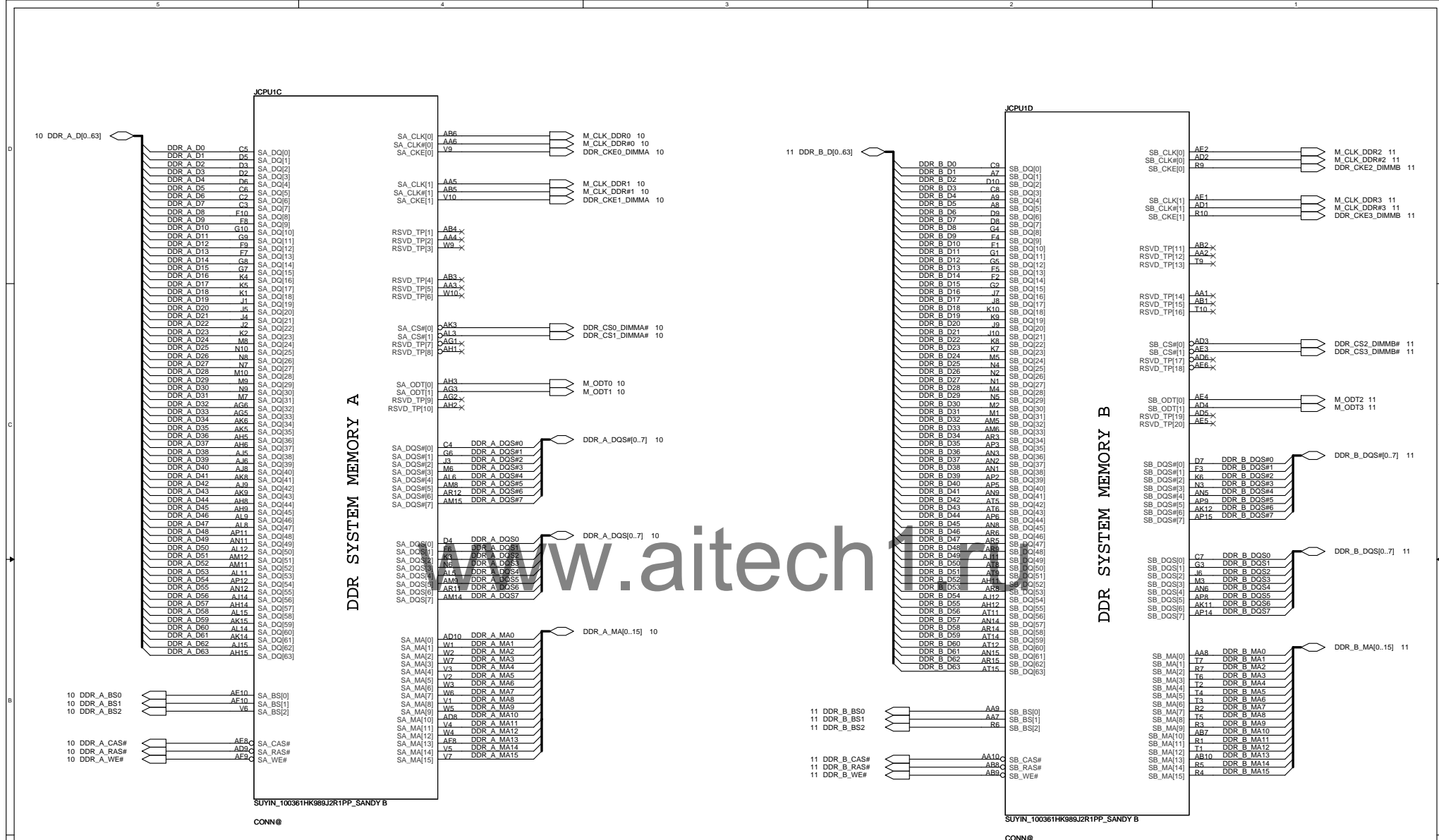
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board id	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	3.3K +/- 5%	0.0908 V	0.1054 V	0.121 V
2	6.8K +/- 5%	0.1817 V	0.2101 V	0.2422 V
3	10K +/- 5%	0.2601 V	0.3 V	0.3448 V
4	15K +/- 5%	0.3746 V	0.4304 V	0.4927 V
5	20K +/- 5%	0.4974 V	0.55 V	0.6076 V
6	NC	2.500 V	3.300 V	3.300 V
7				

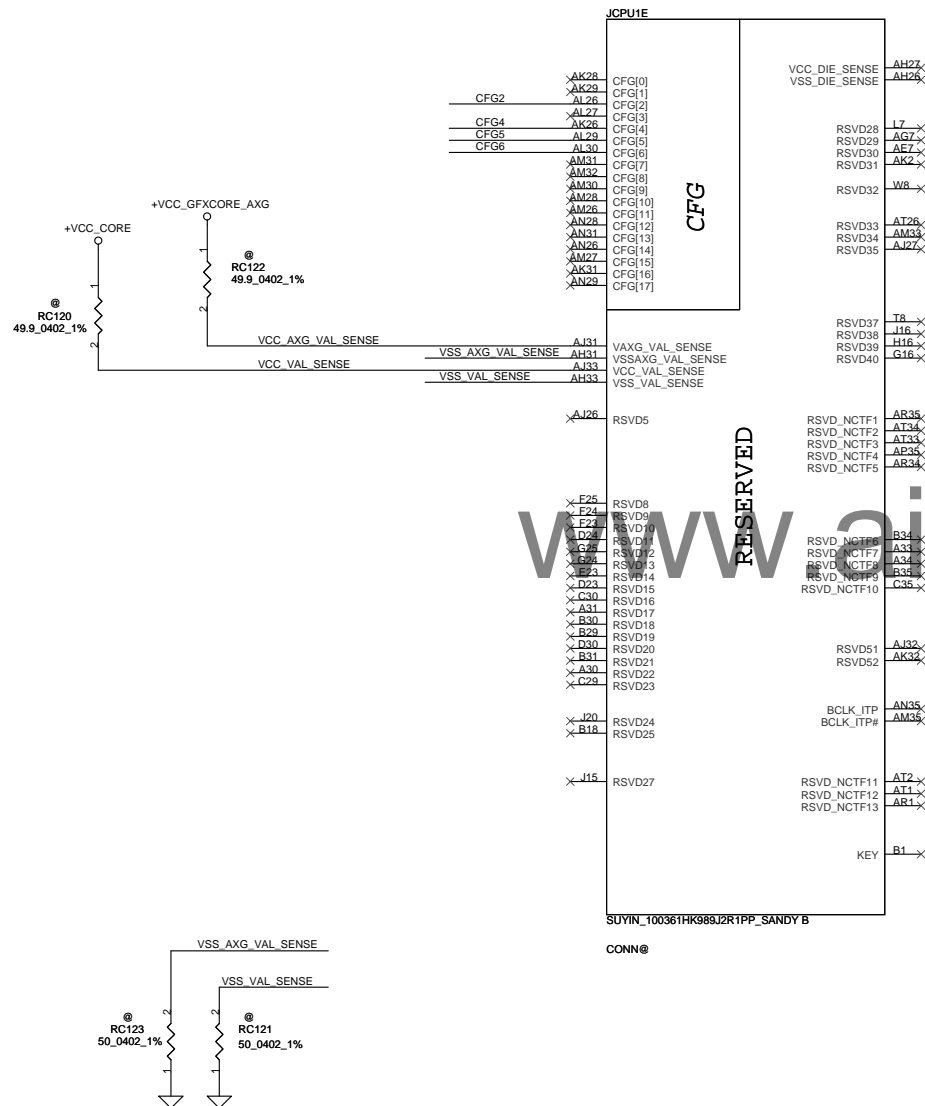
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				Rev	8



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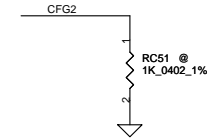


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Date				Sheet	6 of 58

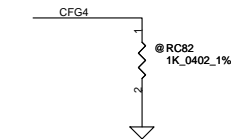


INTEL 12/28 recommend
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1

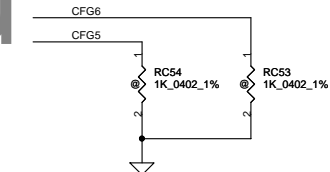
CFG Straps for Processor



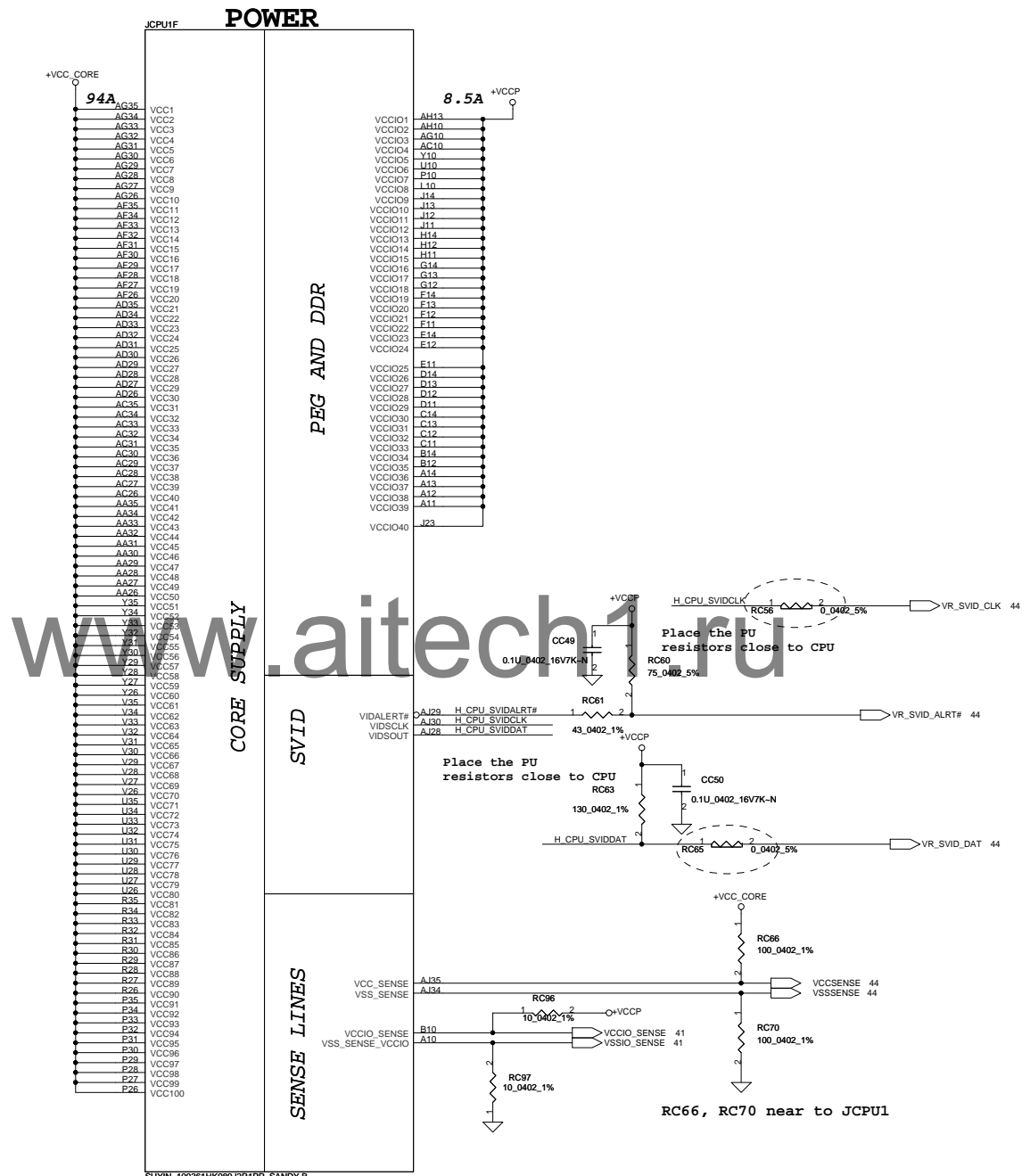
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



SUYIN_100361HK989J2R1PP_SANDY B

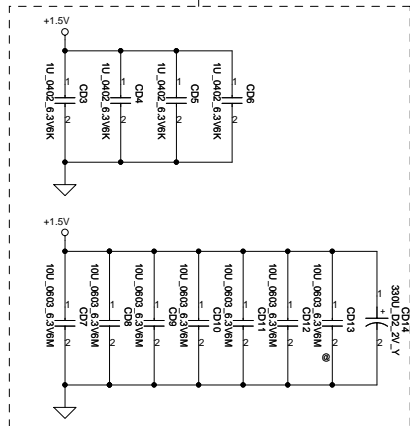
CONN@

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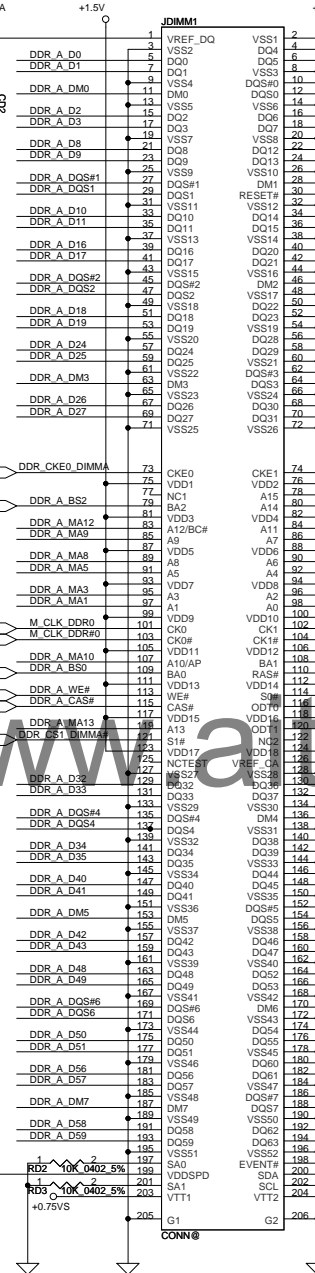
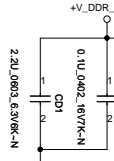
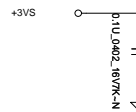
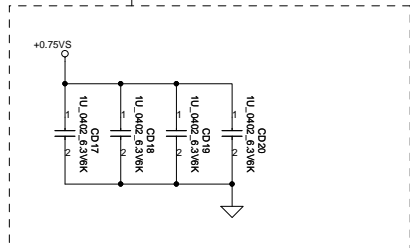
6 DDR_A_DQS#0..7
6 DDR_A_DQS#0..7
6 DDR_A_D[0..63]
6 DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

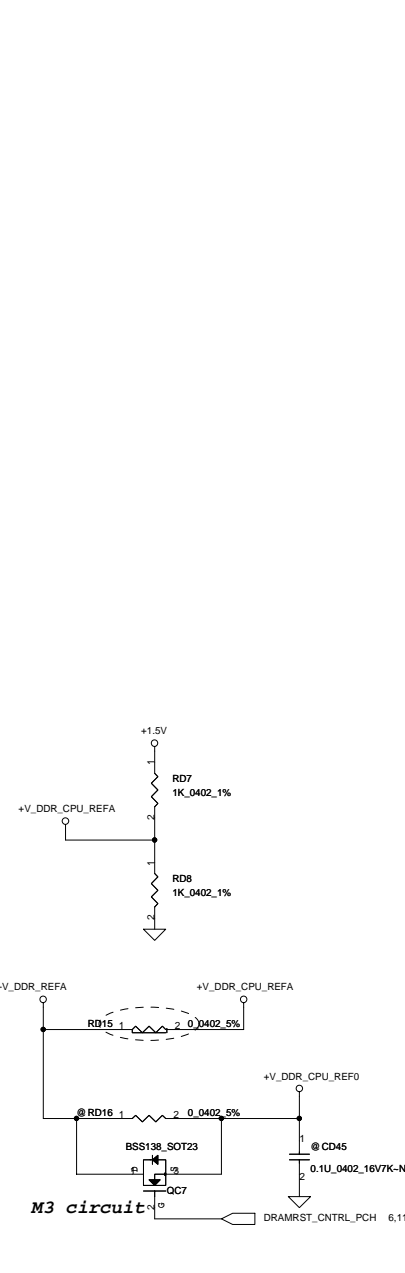
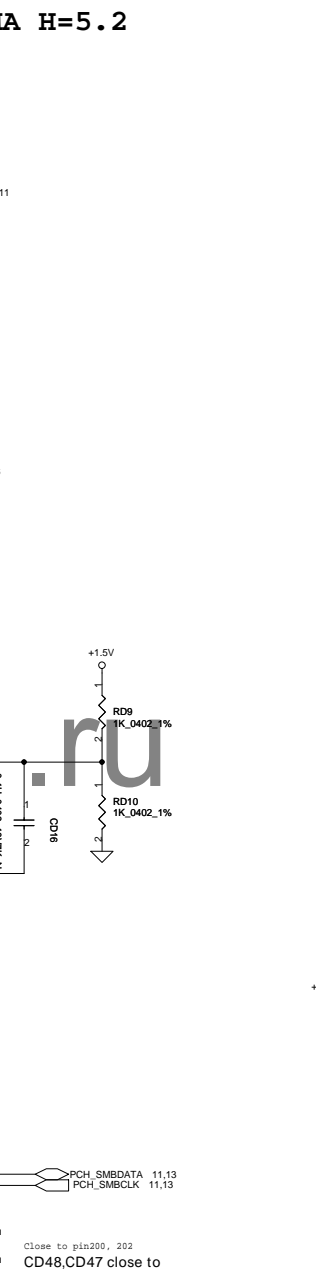
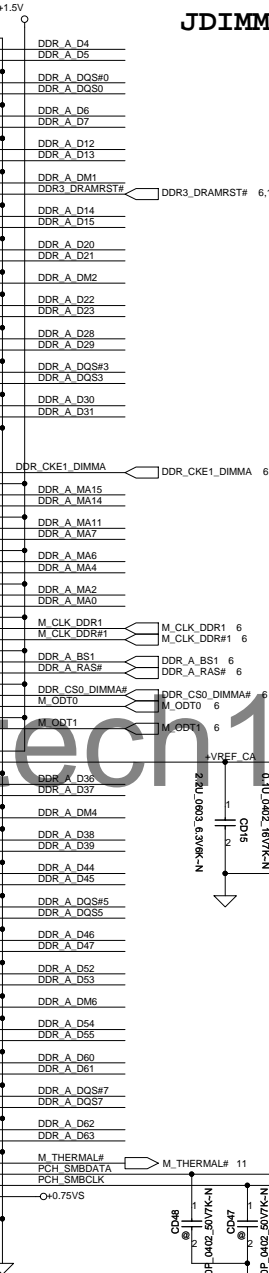
Layout Note:
Place near JDIMM1



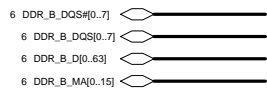
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Place near JDIMM1.203,204



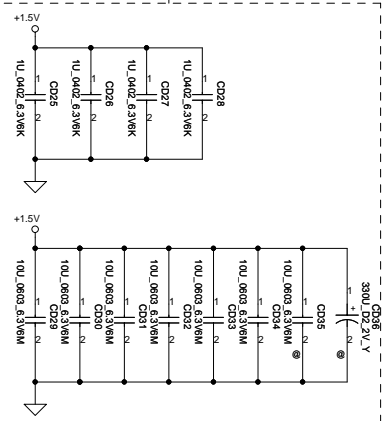
JDIMMA H=5.2



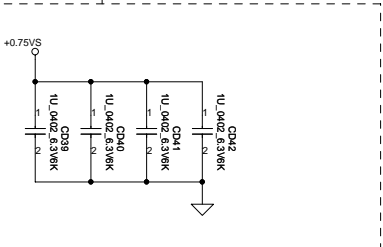
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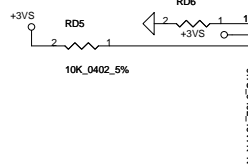
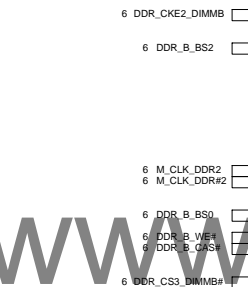
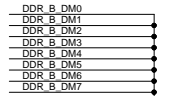
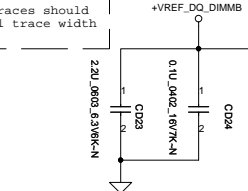
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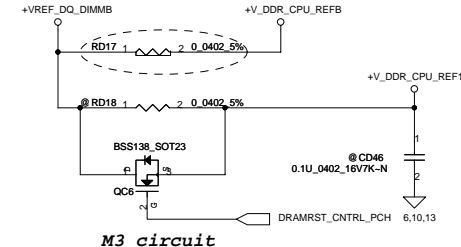
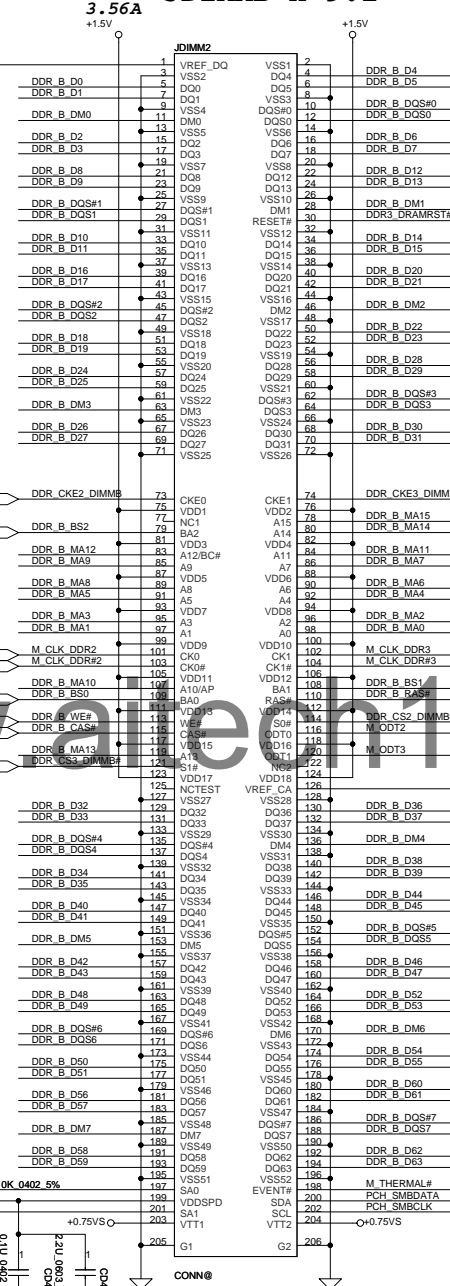
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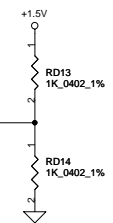
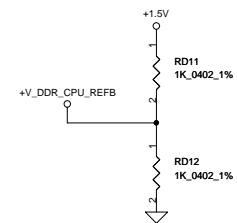
All VREF traces should
have 10 mil trace width



JDIMMB H=9.2

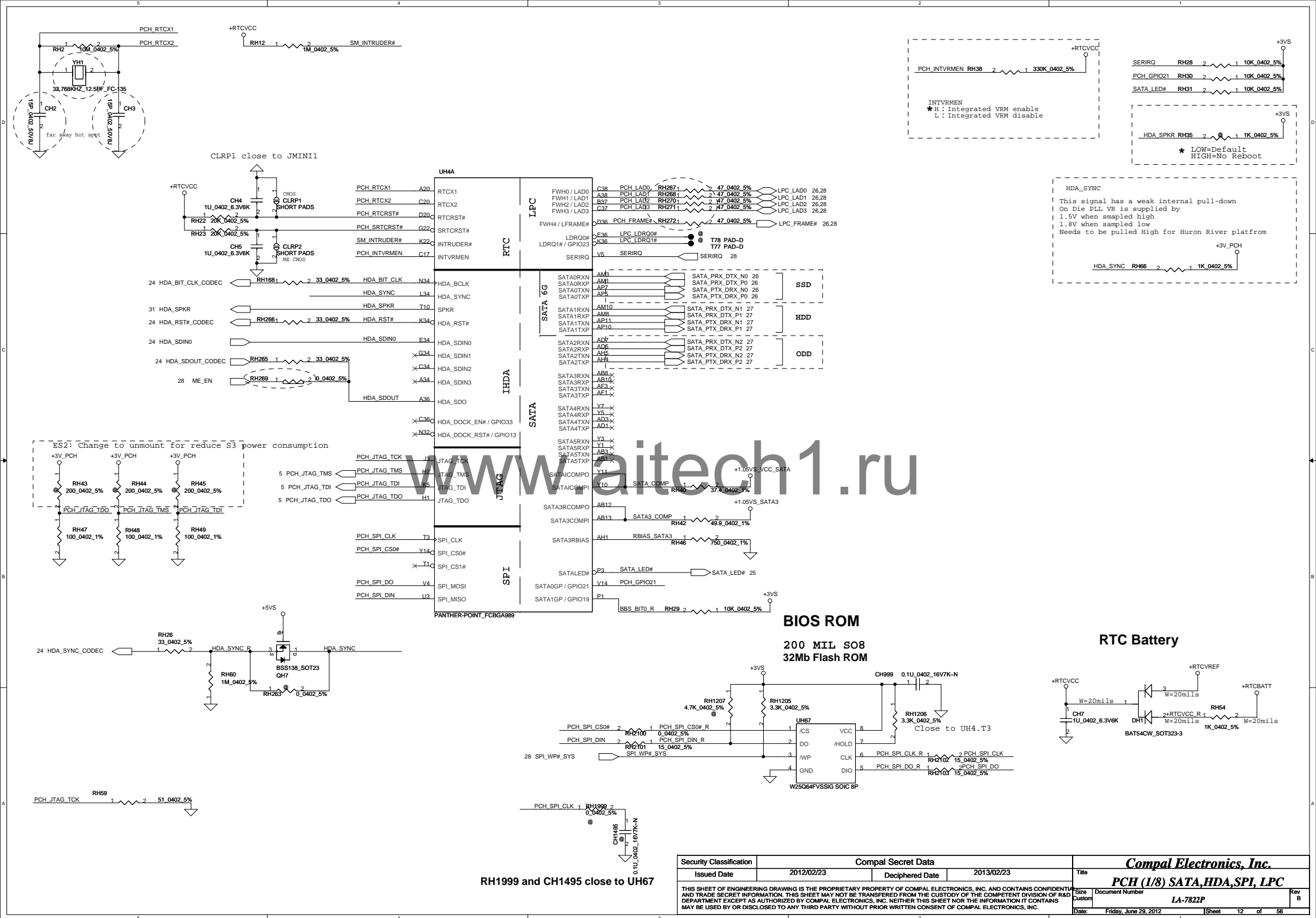


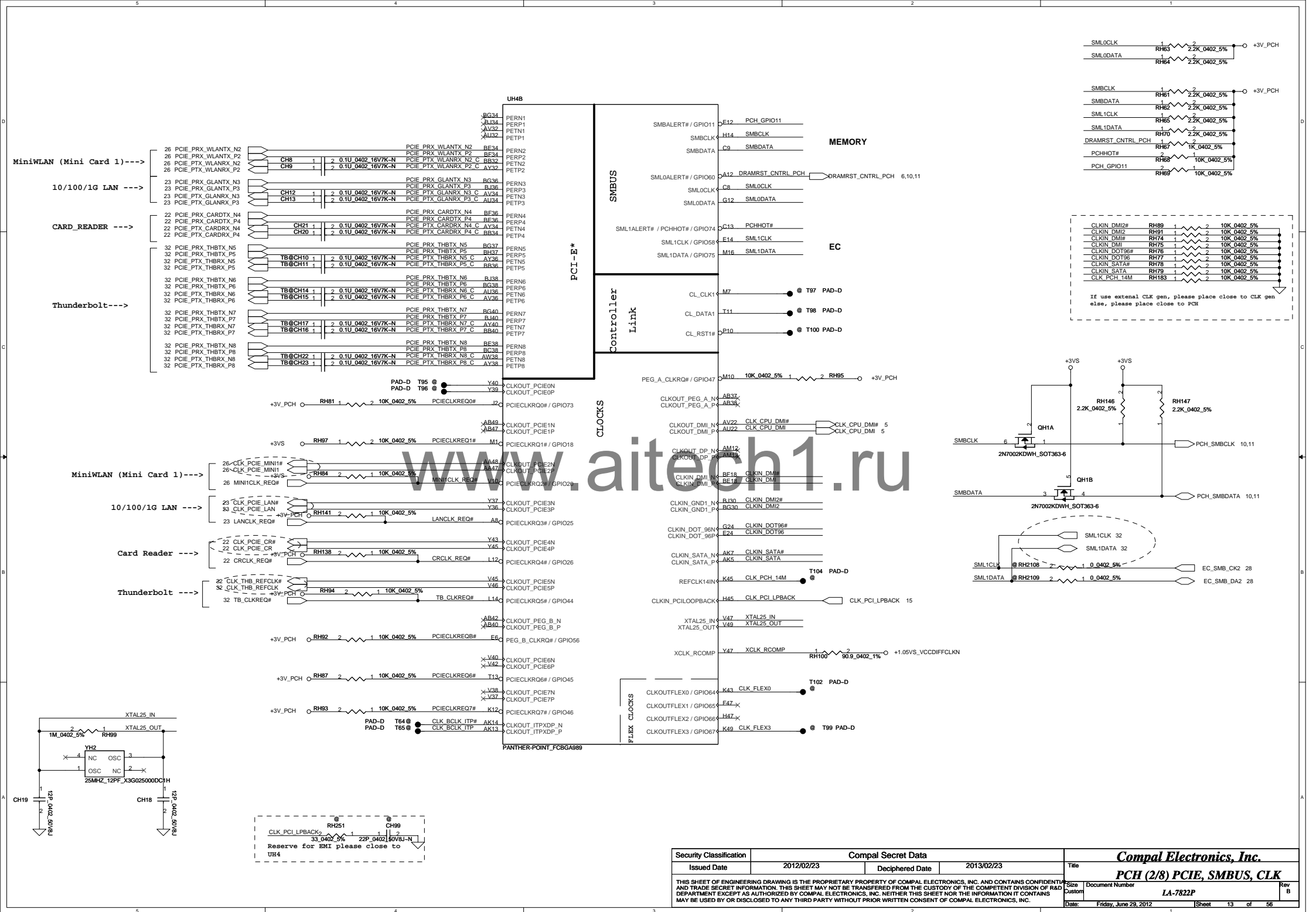
M3 circuit

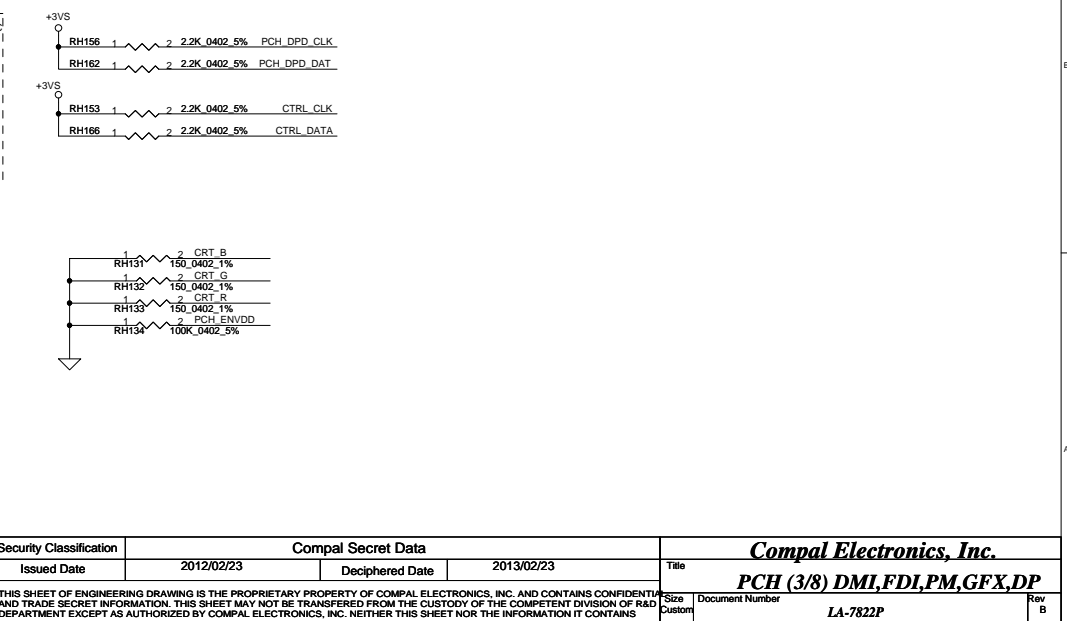
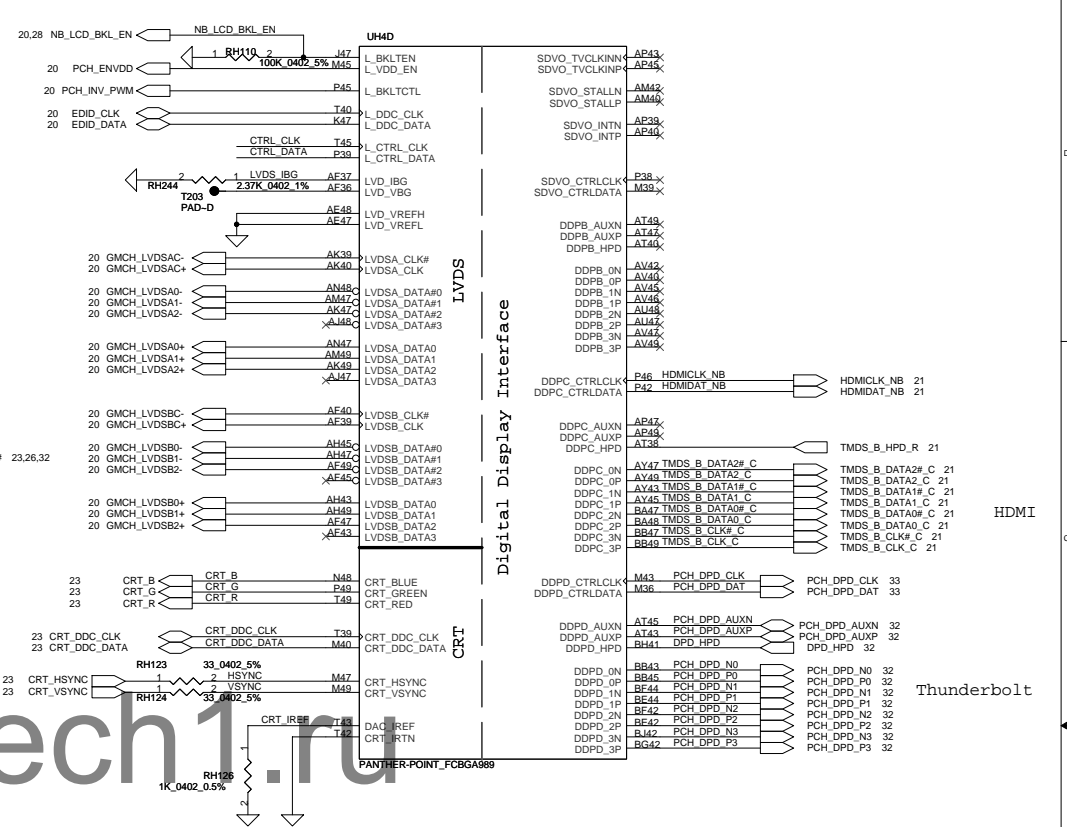
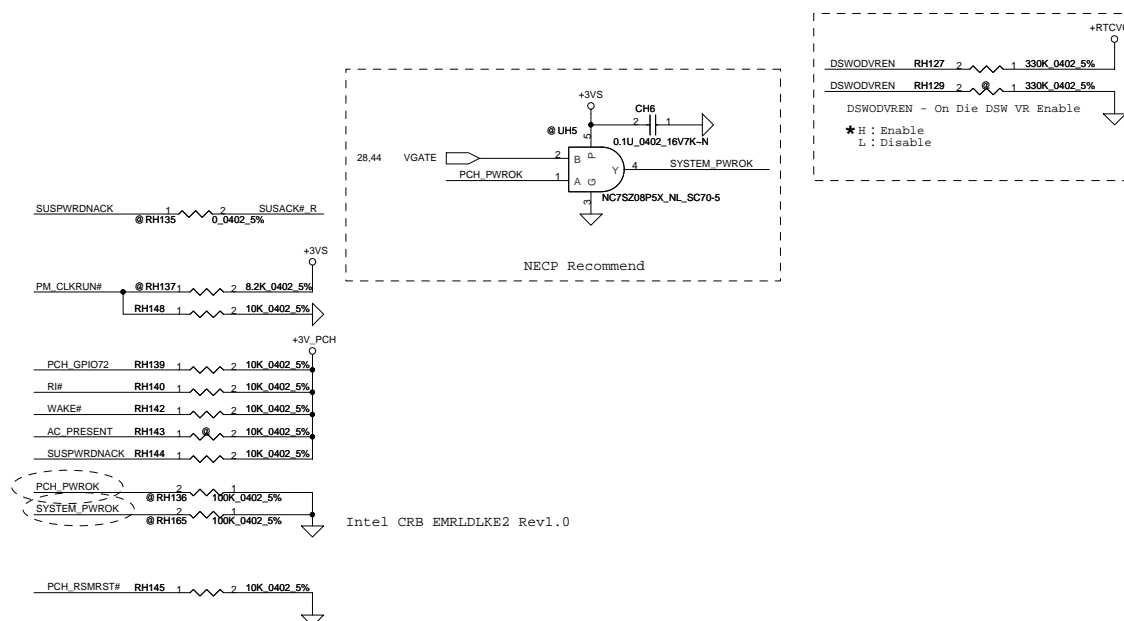
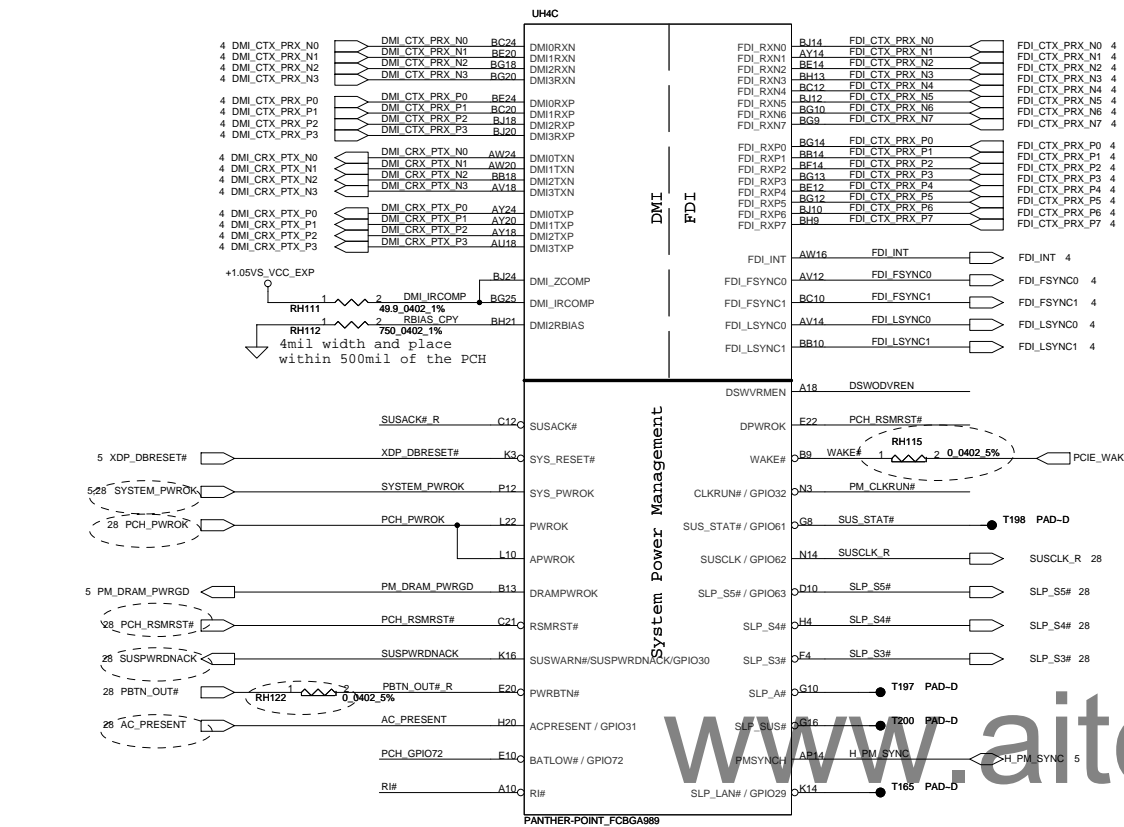


CD49,CD50 close to
PIN200,202

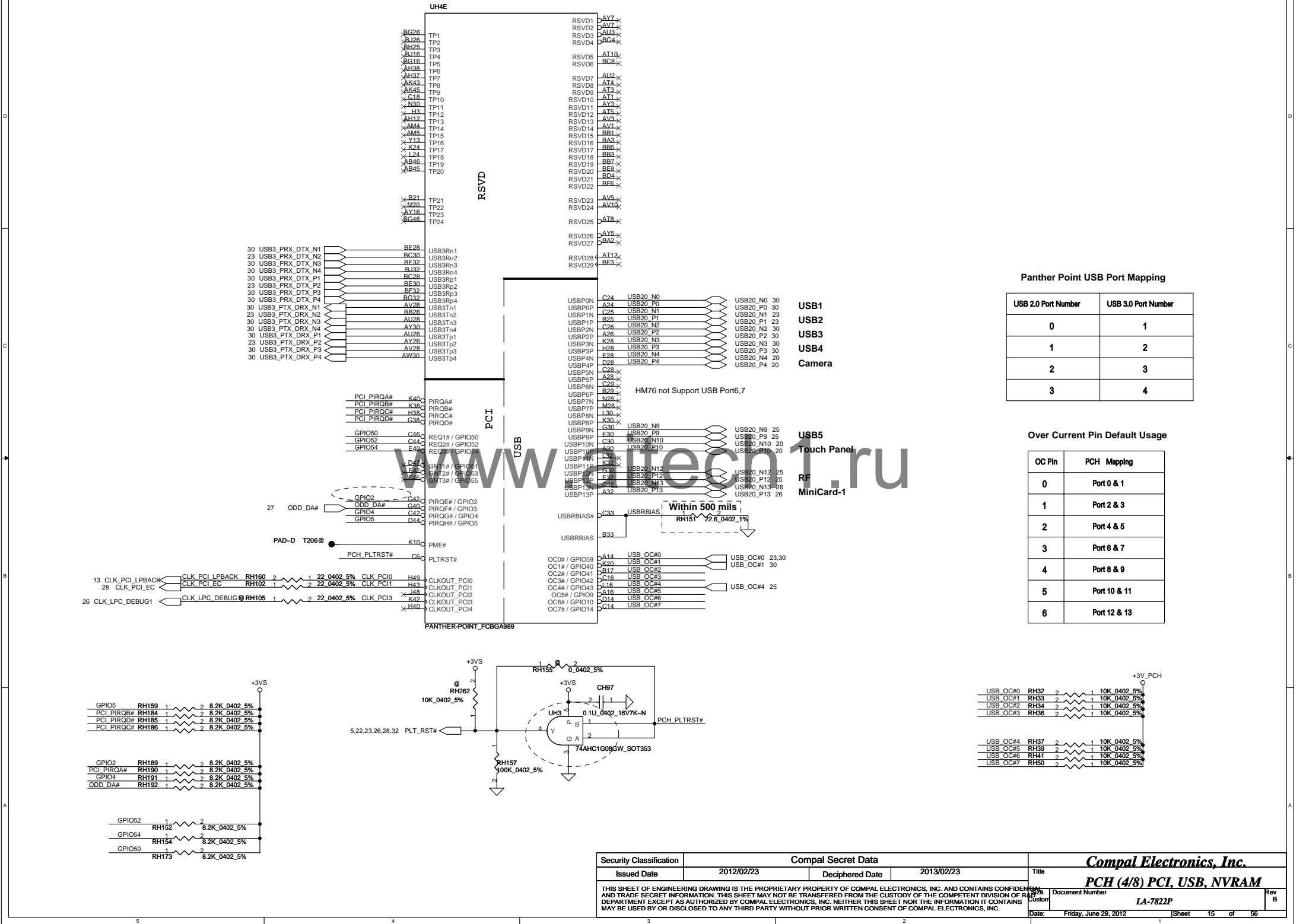
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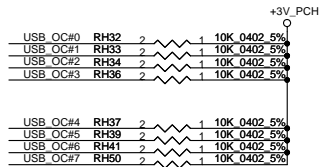


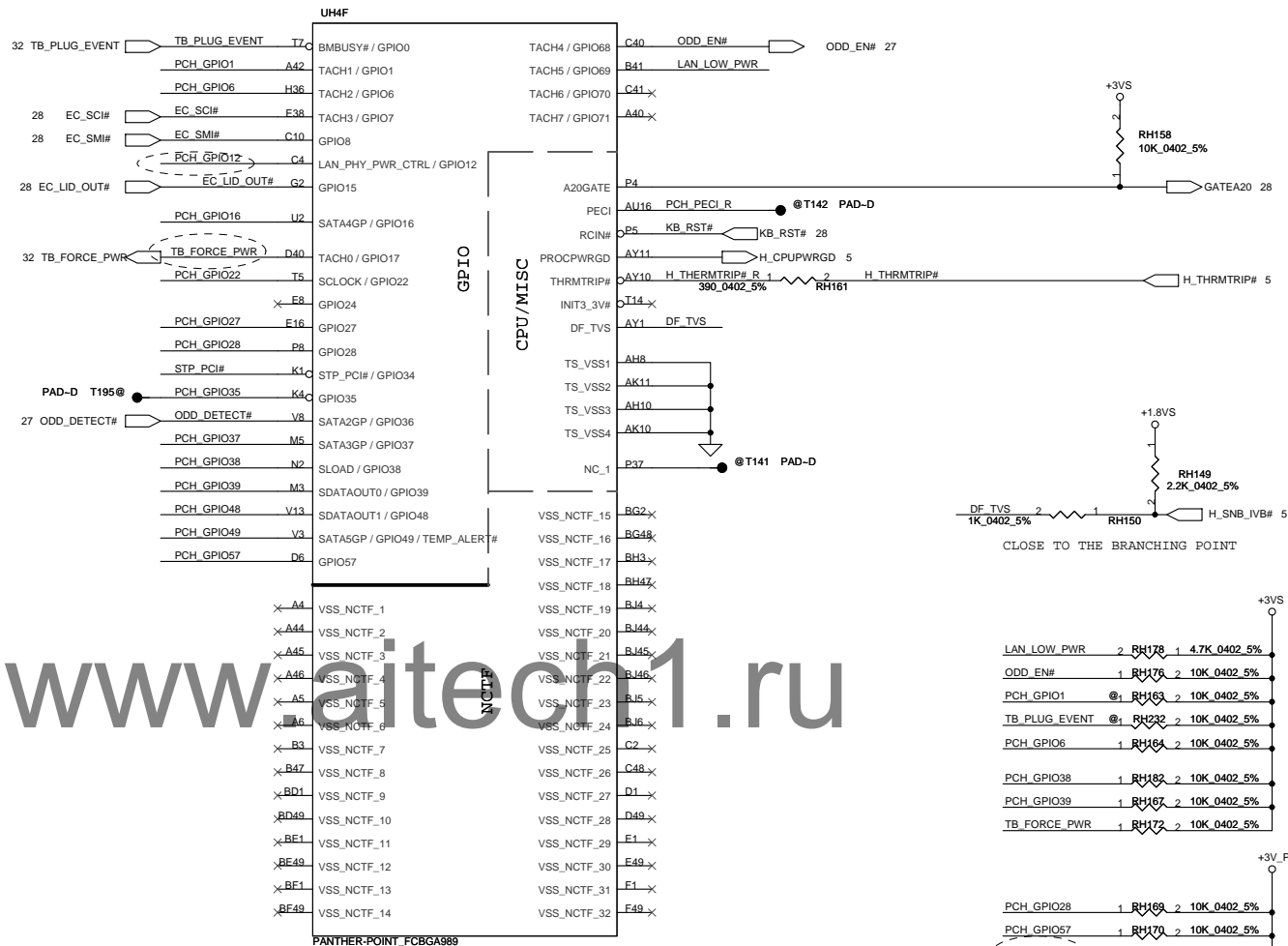
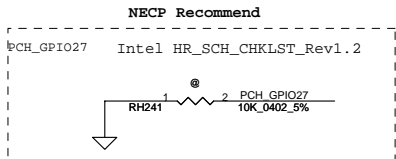
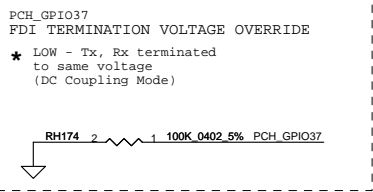
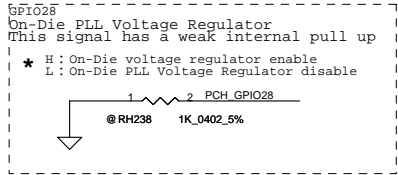
Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

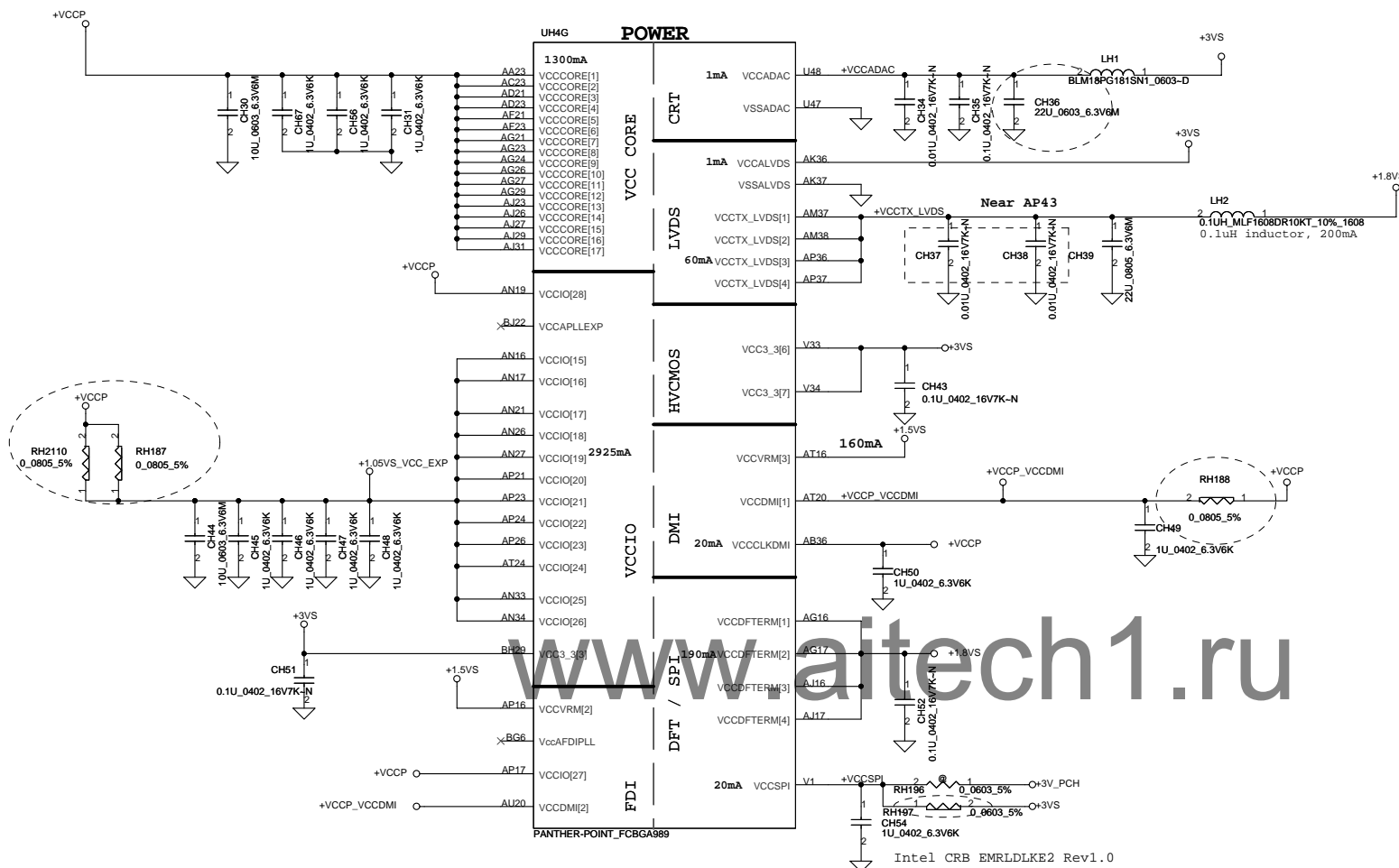
Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13





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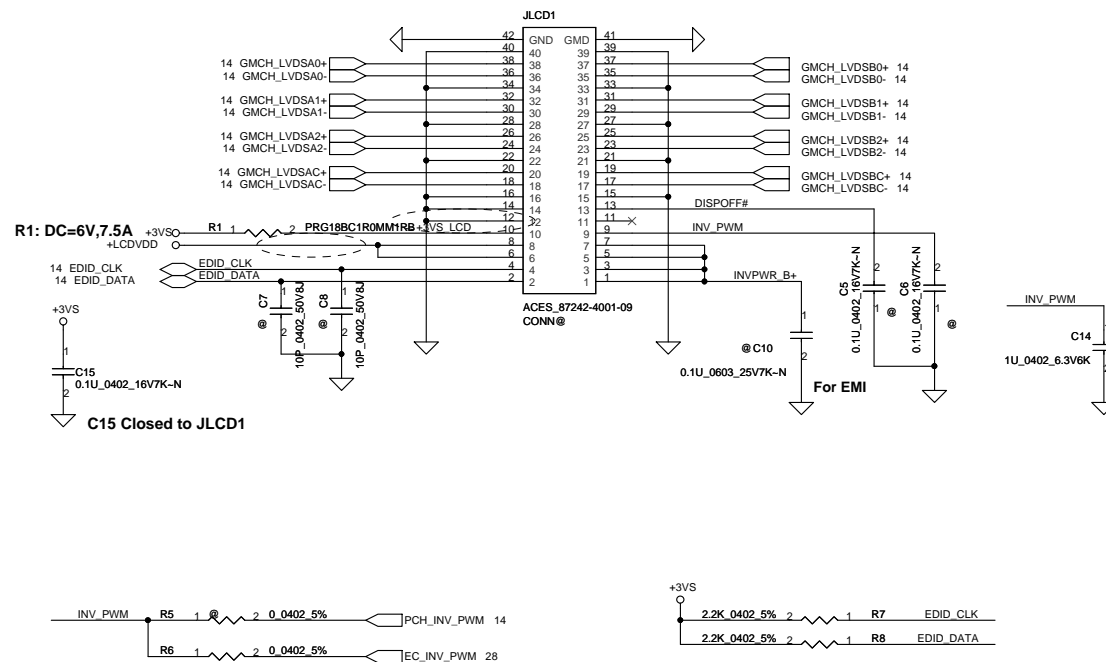


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.002
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.73
VccDMI	1.1	0.047
VccIO	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.147
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04
DcpSus	1.05	0.12

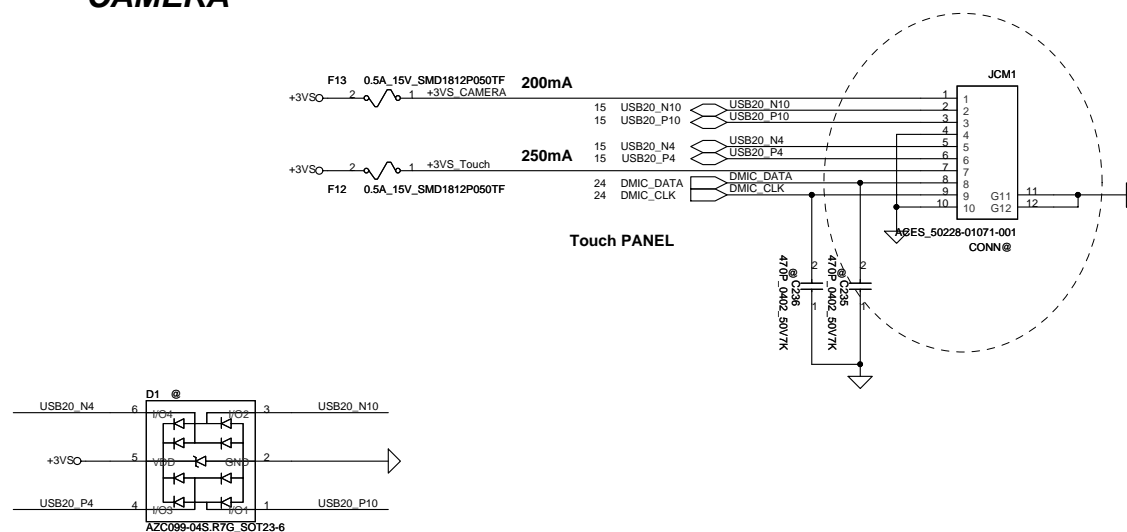


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				Customer	Document Number		Rev B	
					LA-7822P			
				Date:	Friday, June 29, 2012	Sheet 19 of 56		

LCD POWER CIRCUIT



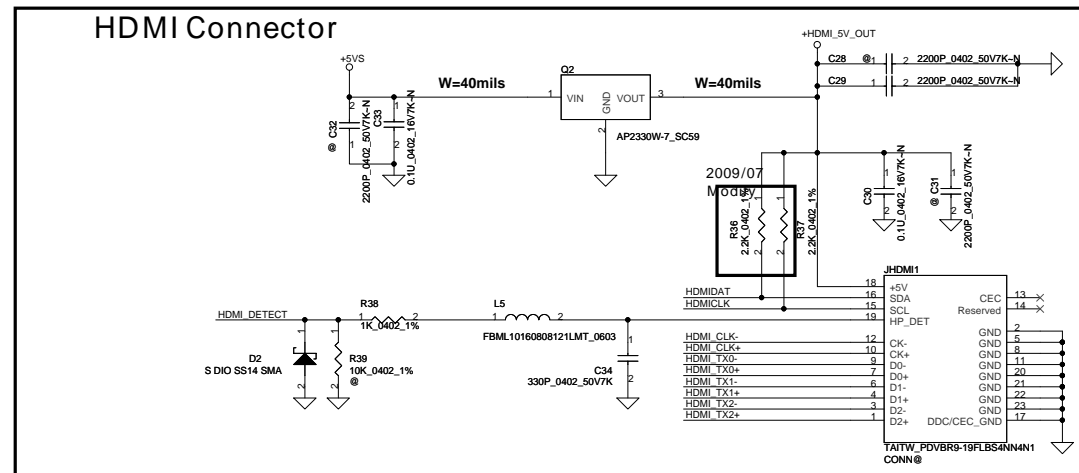
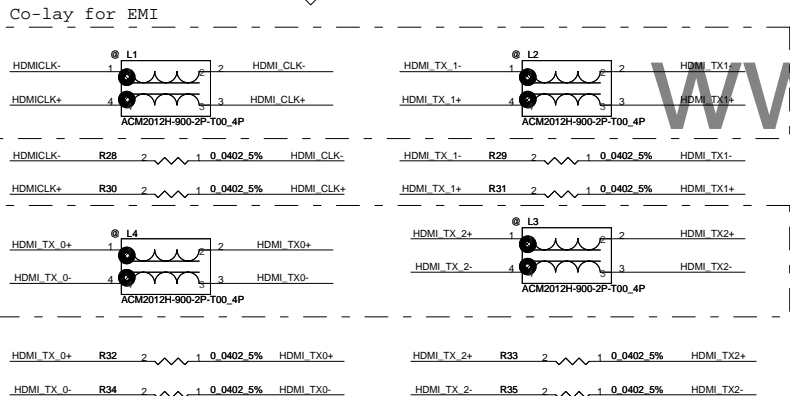
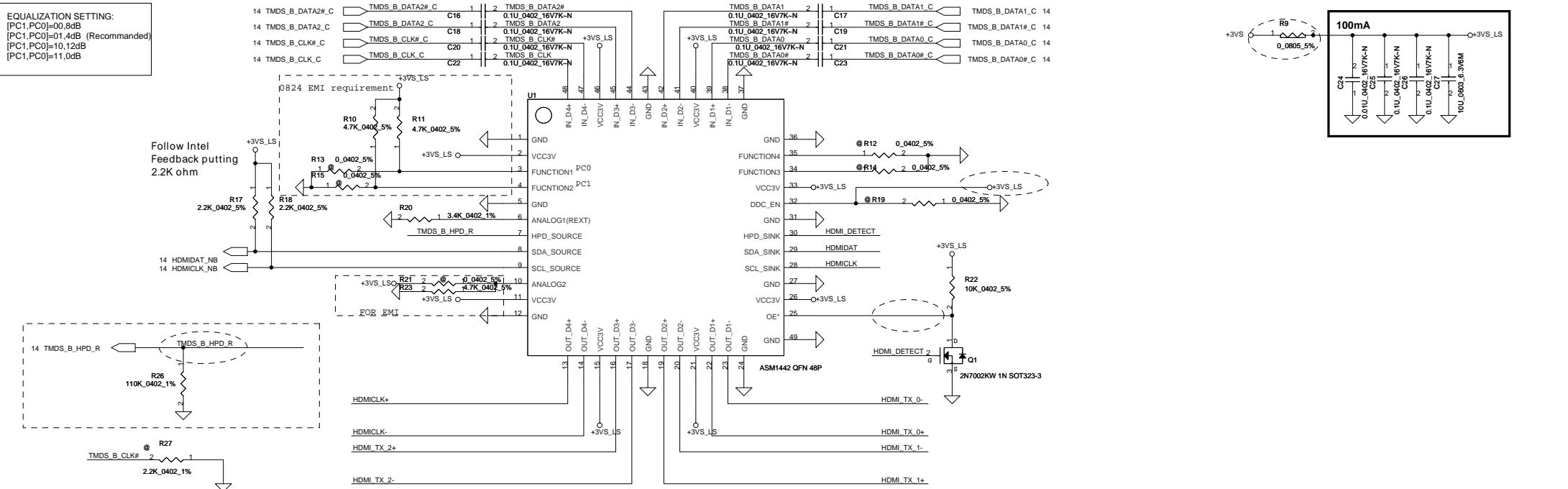
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CAMERA

ESD

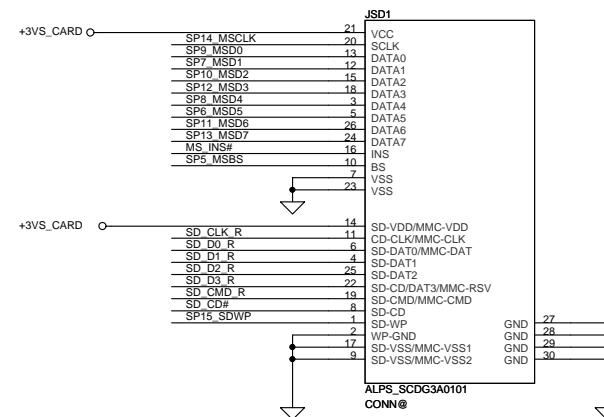
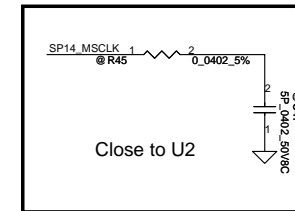
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/02/23	Deciphered Date	2013/02/23	Title	LCD Conn	
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EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommended)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB



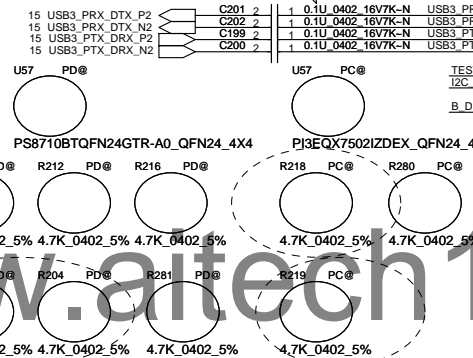
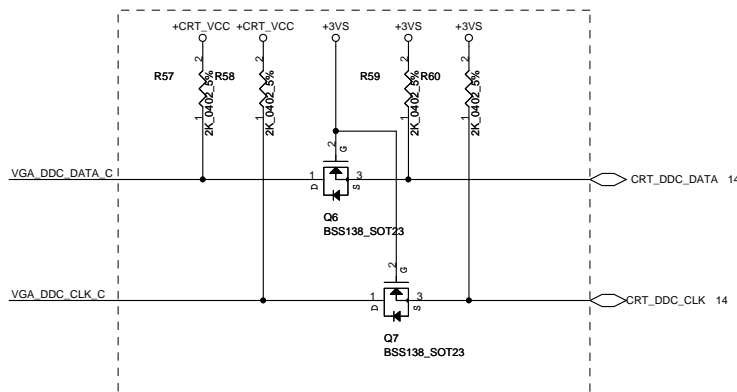
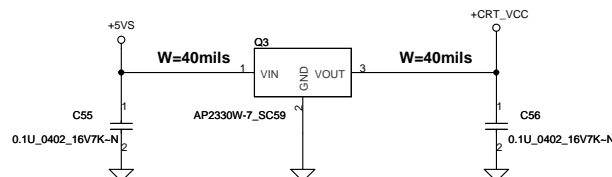
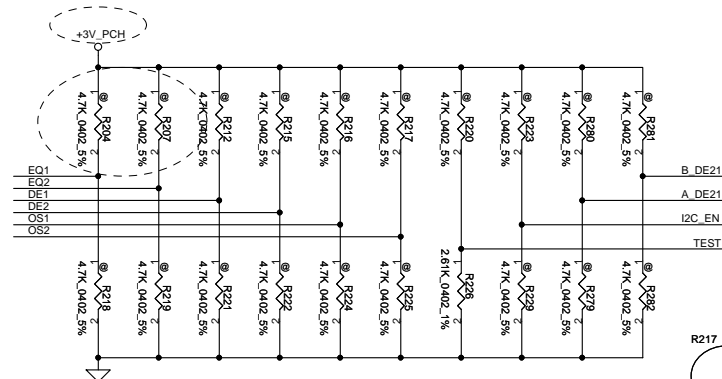
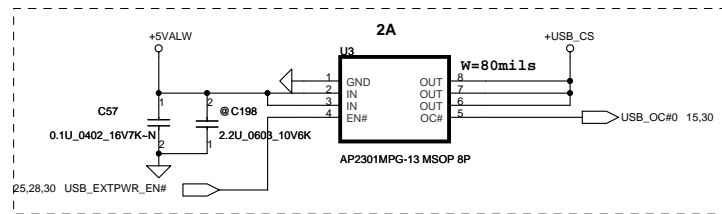
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Issued Date	2012/02/23	Deciphered Date	2013/02/23	Document Number	LA-7822P
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Card Reader

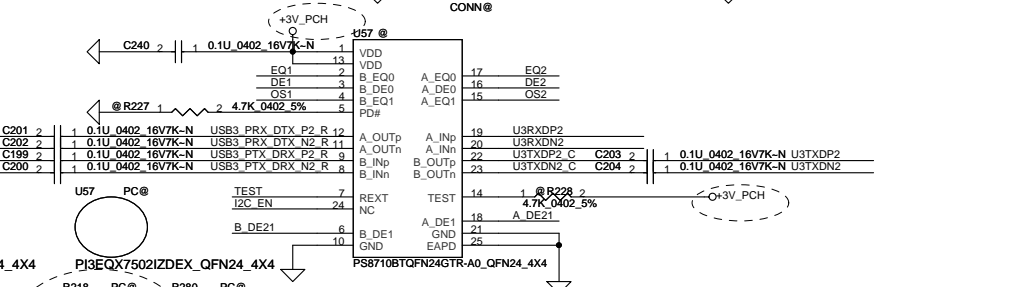
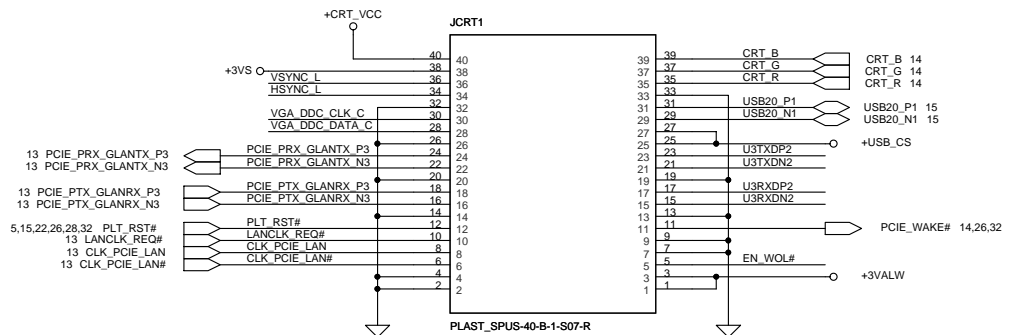


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LAN / CRT CONN

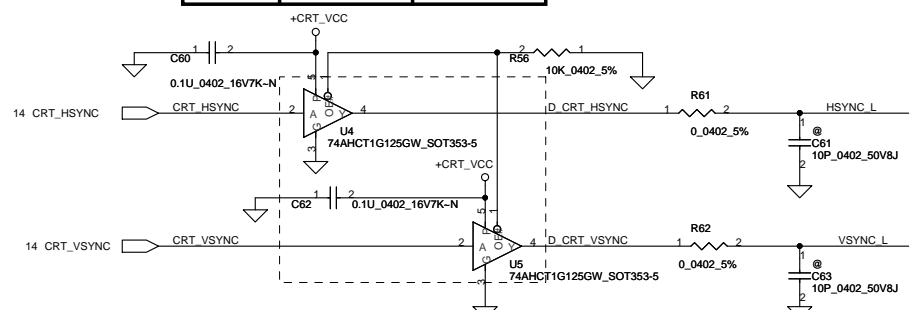


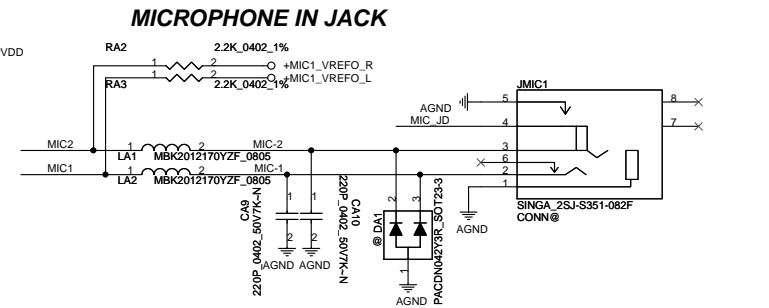
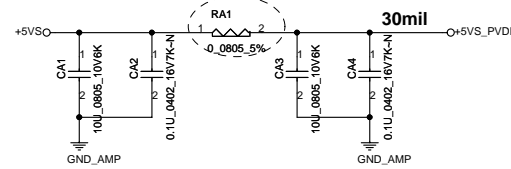
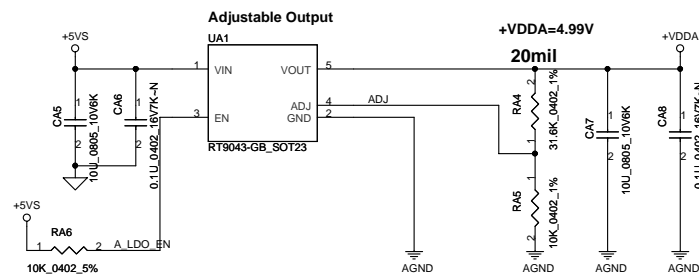
	R212	R216	R280	R281	R218	R219	R204	R207
PD@	4.7K	4.7K	@	4.7K	@	@	4.7K	4.7K
PC@	@	@	4.7K	@	4.7K	4.7K	@	@



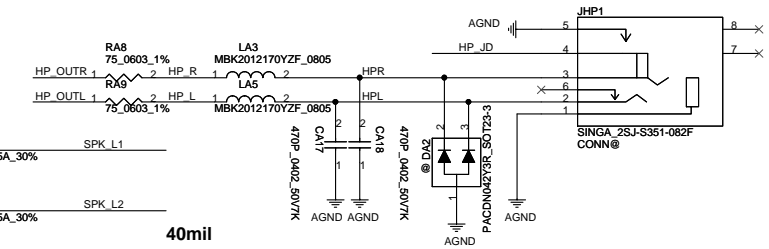
Parade	B channel Port2 (TX)	A channel Port2 (RX)
DE	5 dB B_DE0 / A_DE0 (H L)	3.5 dB A_DE1 / A_DE0 (L L)
EQ	11.5 dB B_EQ0 / B_EQ0 (H H)	11.5 dB A_EQ0 / A_EQ0 (H H)

Pericom	B channel Port2 (TX)	A channel Port2 (RX)
DE	-3.5 dB B_DE0 (open)	-3.5 dB A_DE0 (open)
EQ	3 dB B_EQ0 (0)	3 dB A_EQ0 (0)

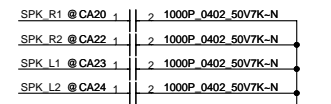




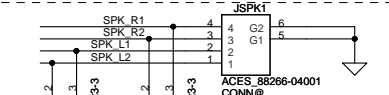
HEADPHONE OUT JACK



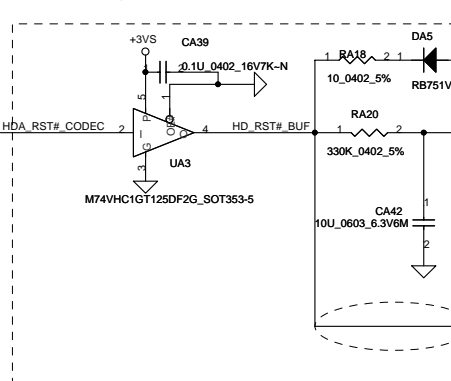
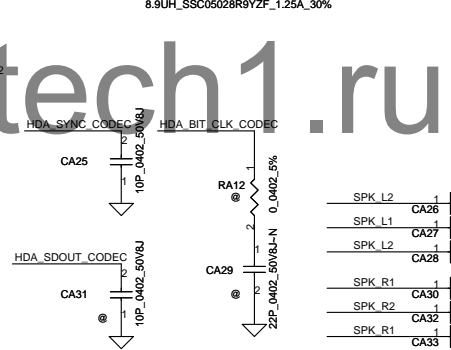
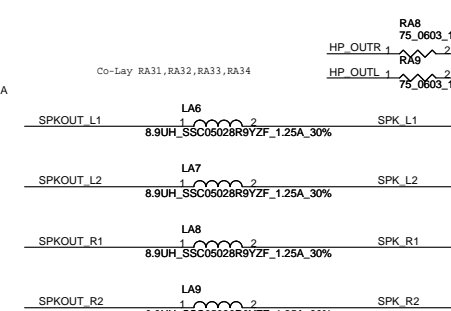
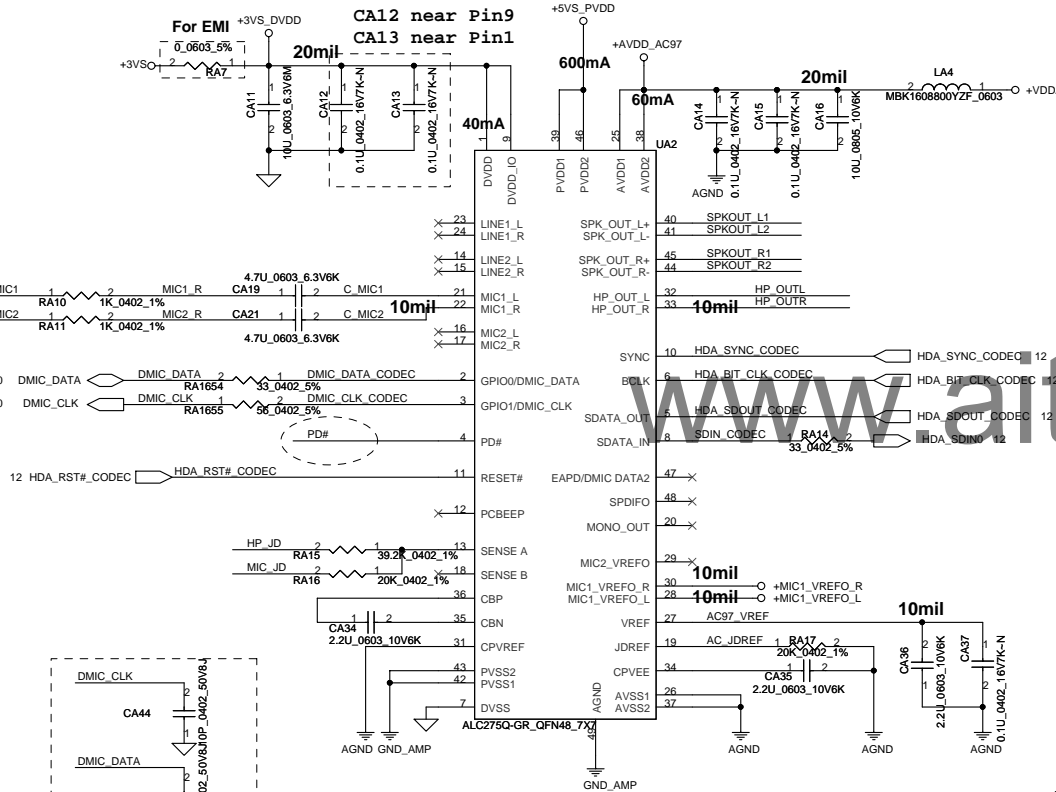
Speaker Connector



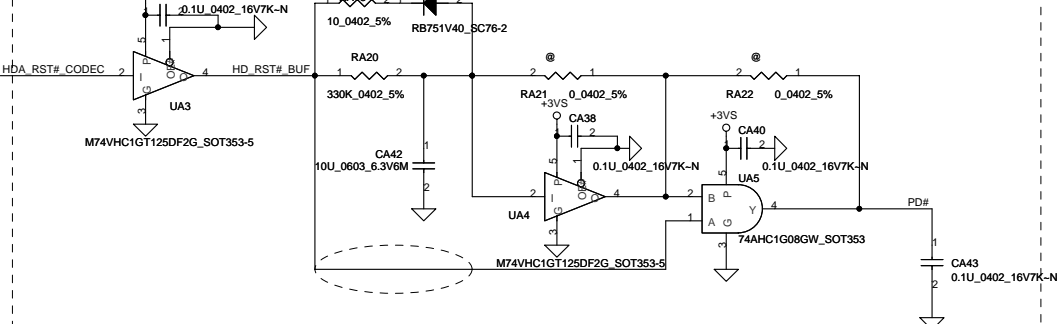
2009/11/02 Modify



NECP Recommend

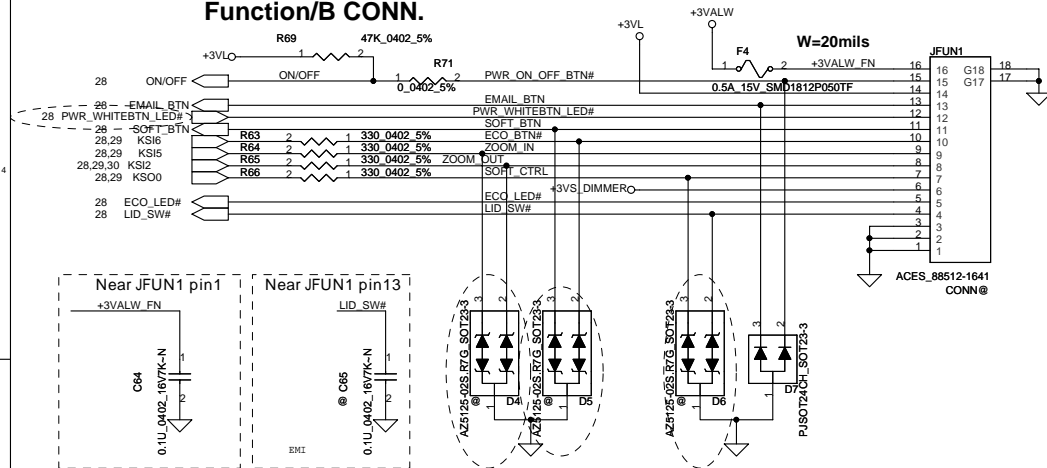


EAPD Control for Vista

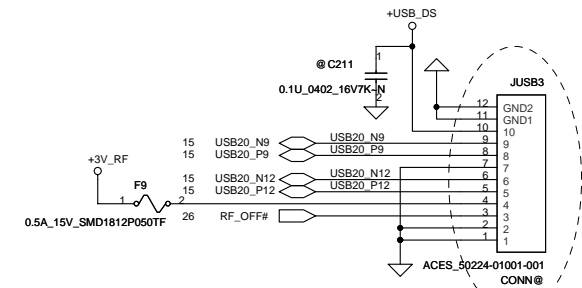
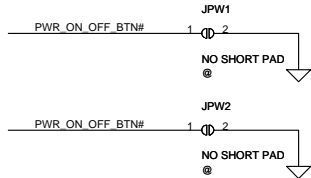
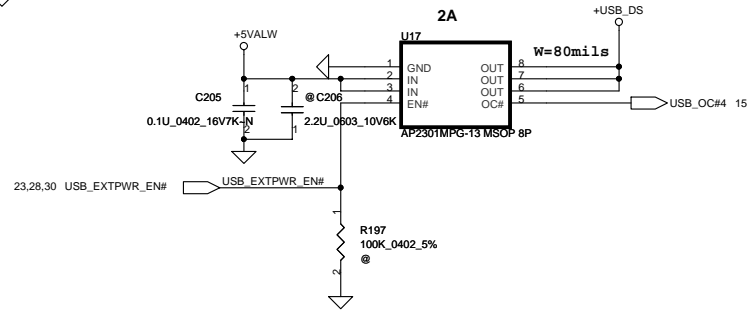


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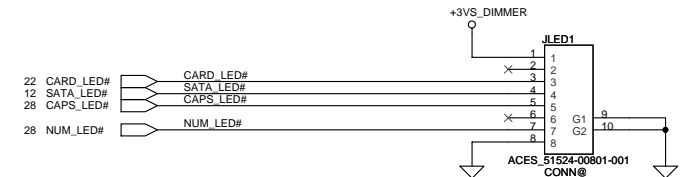
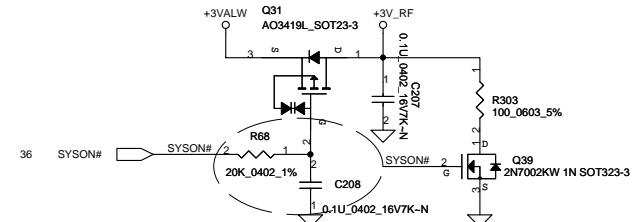
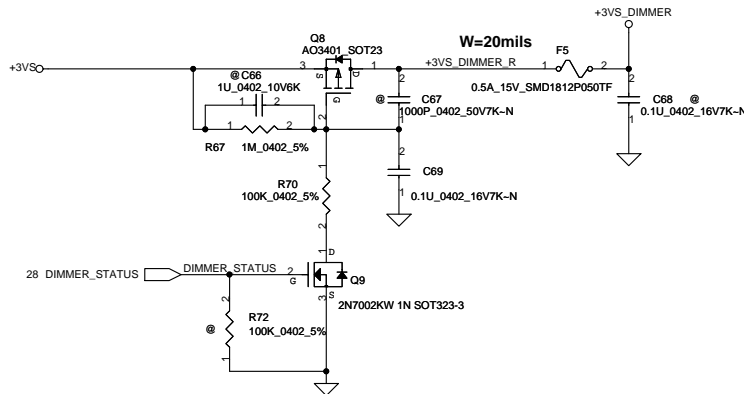
Function/B CONN.



USB2.0/B CONN.



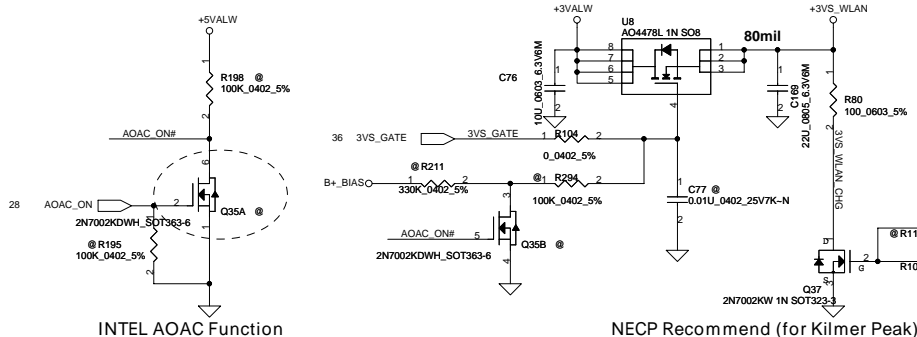
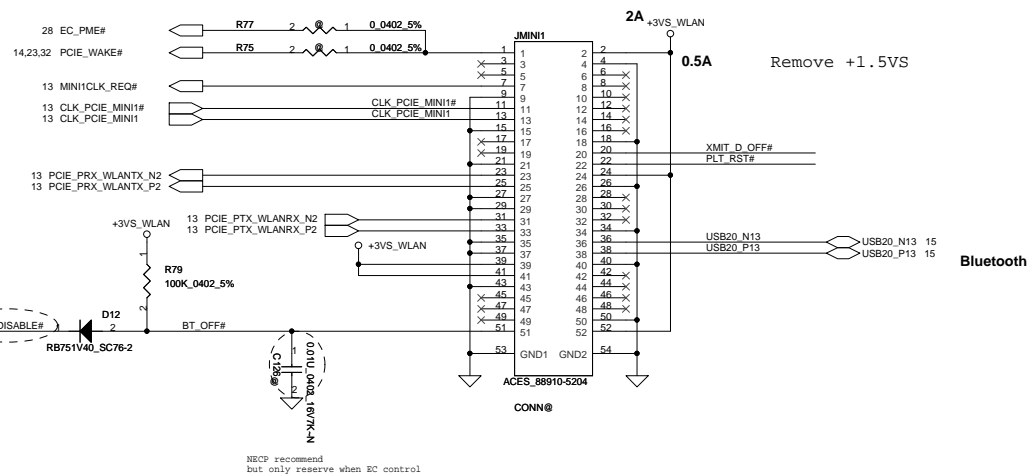
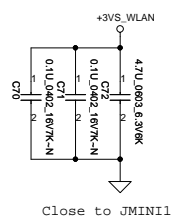
LED Circuit



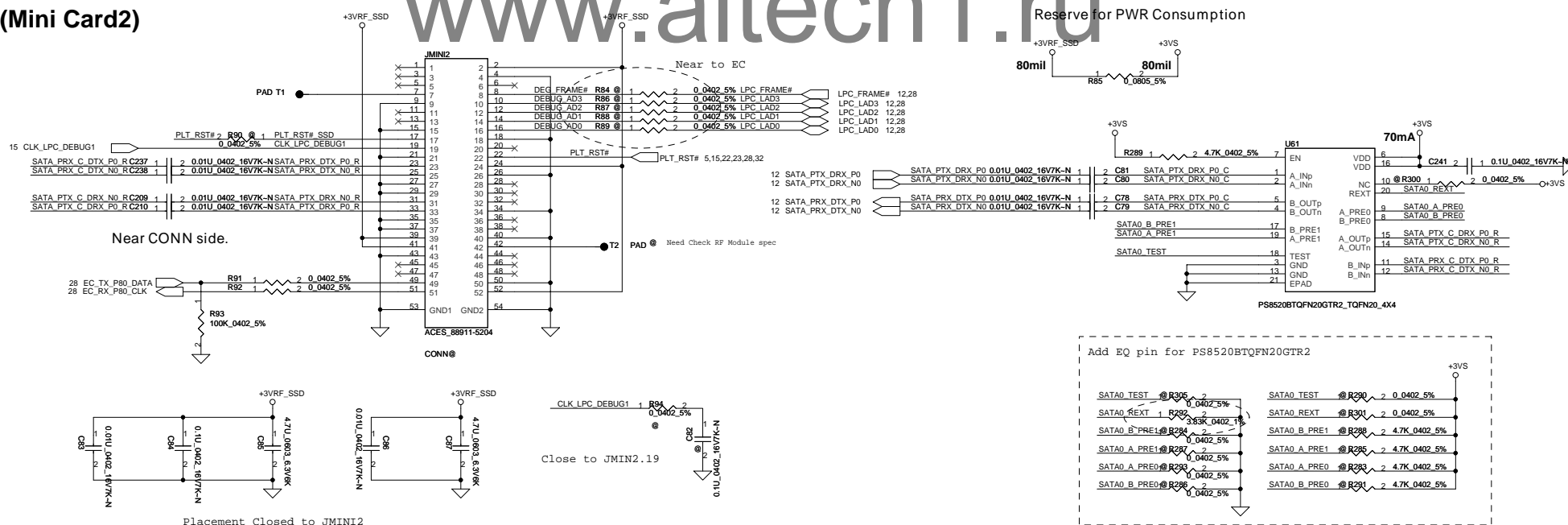
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Killer switch



NECP Recommend (for Kilmer Peak)



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					Custom	LA-7822P	B	
Date:					Friday, June 29, 2012	Sheet	26	of 56

SATA HDD CONN.

Pinout details for JHDD1:

- 1: GND
- 2: SATA PTX, DRX P1 C
- 3: SATA PTX, DRX N1 C
- 4: SATA PRX, DTX N1 C
- 5: SATA PRX, DTX P1 C
- 6: TX+
- 7: TX-
- 8: 3.3V
- 9: 3.3V
- 10: GND
- 11: 3.3V
- 12: GND
- 13: 5V
- 14: 5V
- 15: GND
- 16: 5V
- 17: GND
- 18: 5V
- 19: GND
- 20: 12V
- 21: 12V
- 22: GND
- 23: GND
- 24: GND

Near CONN side.

Place near HDD CONN

HDD-SATA Redriver

IC: PS8520BTQFN20GTR2_4x4

Place caps. near U60

Add EQ pin for PS8520BTQFN20GTR2

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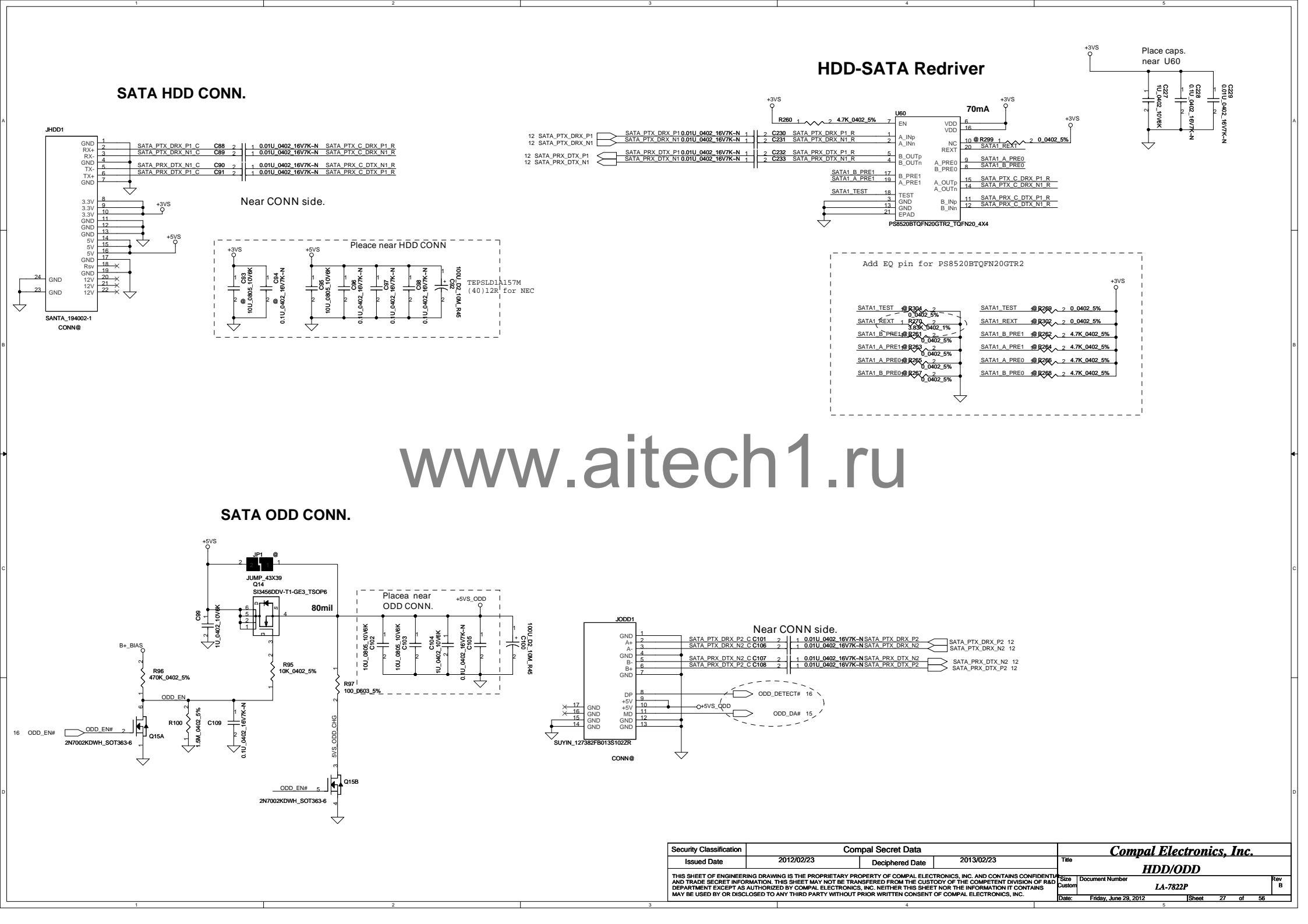
SATA ODD CONN.

Place near ODD CONN.

Pinout details for JODD1:

- 1: GND
- 2: SATA PTX, DRX P2 C
- 3: SATA PTX, DRX N2 C
- 4: SATA PRX, DTX N2 C
- 5: SATA PRX, DTX P2 C
- 6: B+
- 7: B-
- 8: DP
- 9: +5V
- 10: +5V
- 11: MD
- 12: GND
- 13: GND
- 14: GND
- 15: ODD_DETECT#
- 16: ODD_DA#

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SATA HDD CONN.

HDD-SATA Redriver

Place caps. near U60

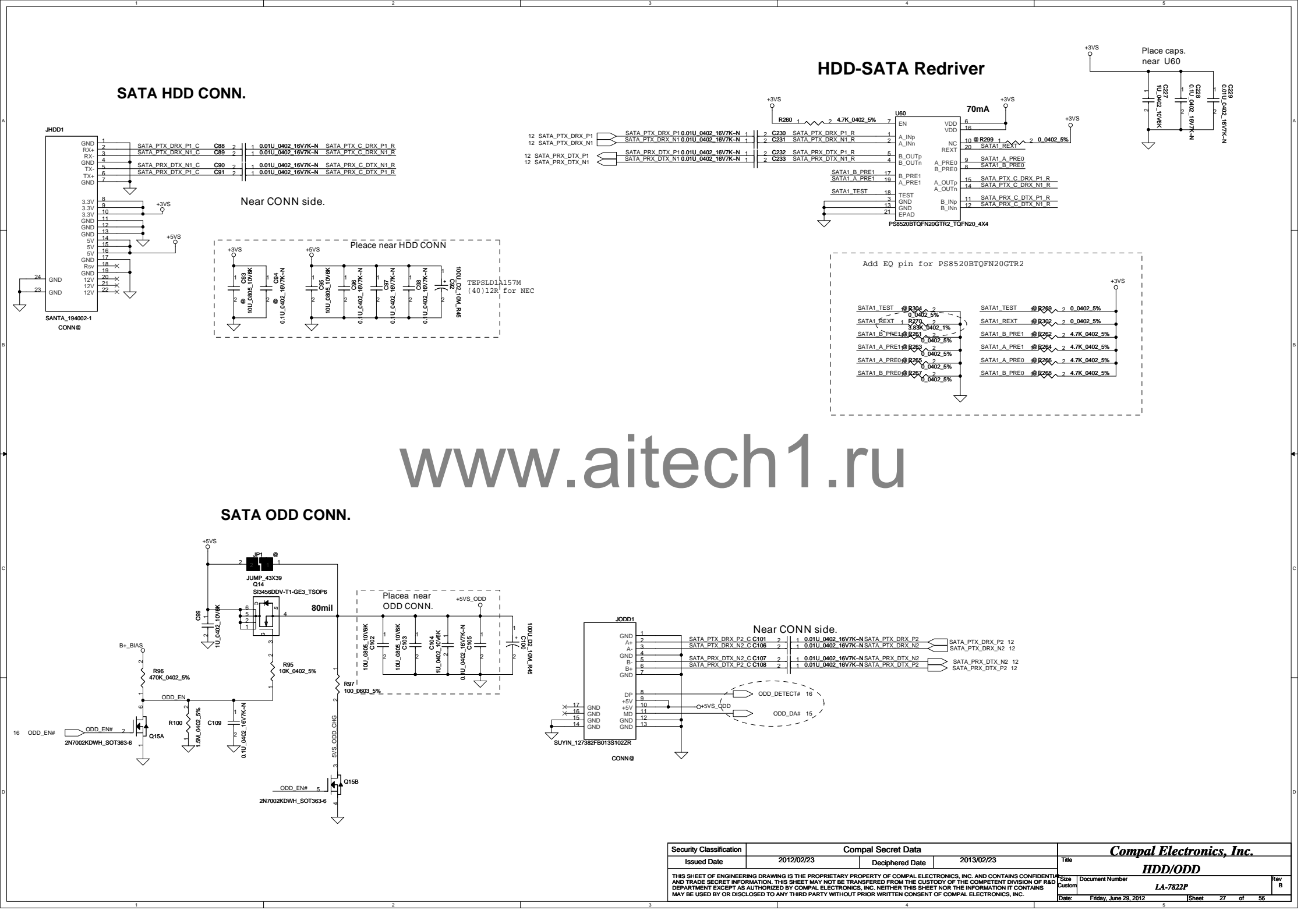
70mA

Add EQ pin for PS8520BTQFN20GTR2

SATA ODD CONN.

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				HDD/ODD	
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SATA HDD CONN.

Near CONN side.

Place near HDD CONN

Place caps. near U60

HDD-SATA Redriver

70mA

Add EQ pin for PS8520BTQFN20GTR2

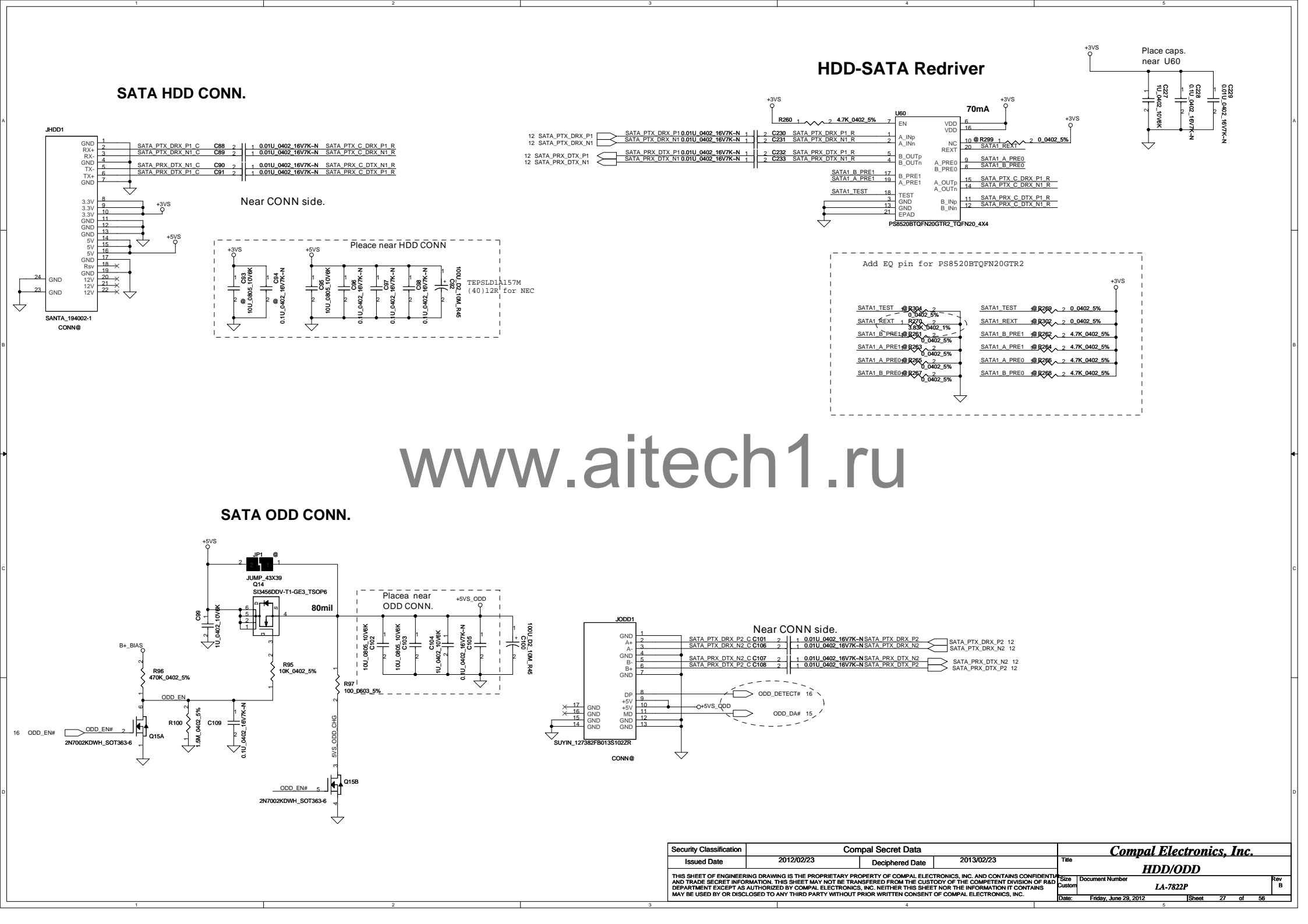
SATA ODD CONN.

Placea near ODD CONN.

Near CONN side.

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SATA HDD CONN.

Near CONN side.

Place near HDD CONN

HDD-SATA Redriver

Place caps. near U60

Add EQ pin for PS8520BTQFN20GTR2

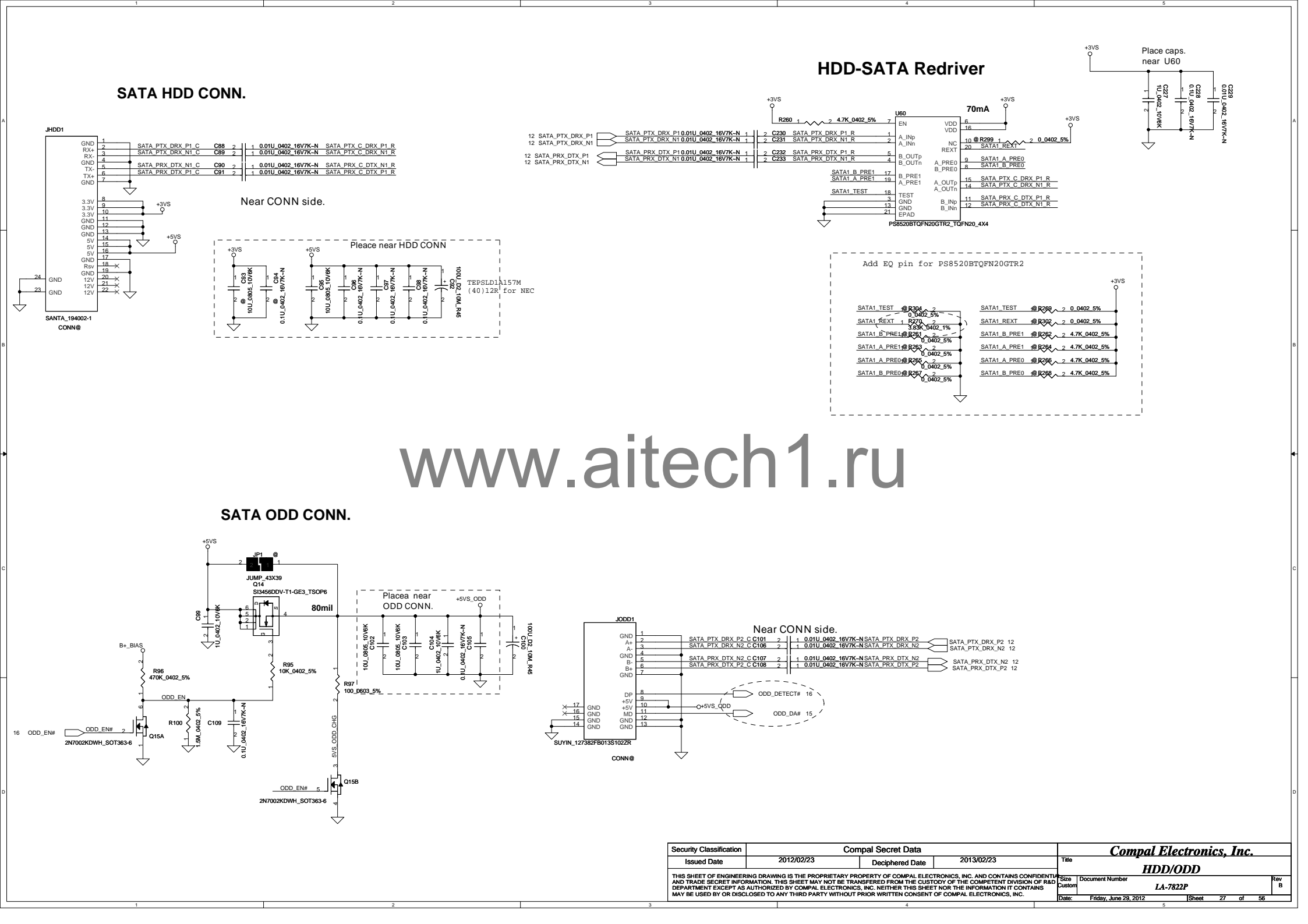
SATA ODD CONN.

Placea near ODD CONN.

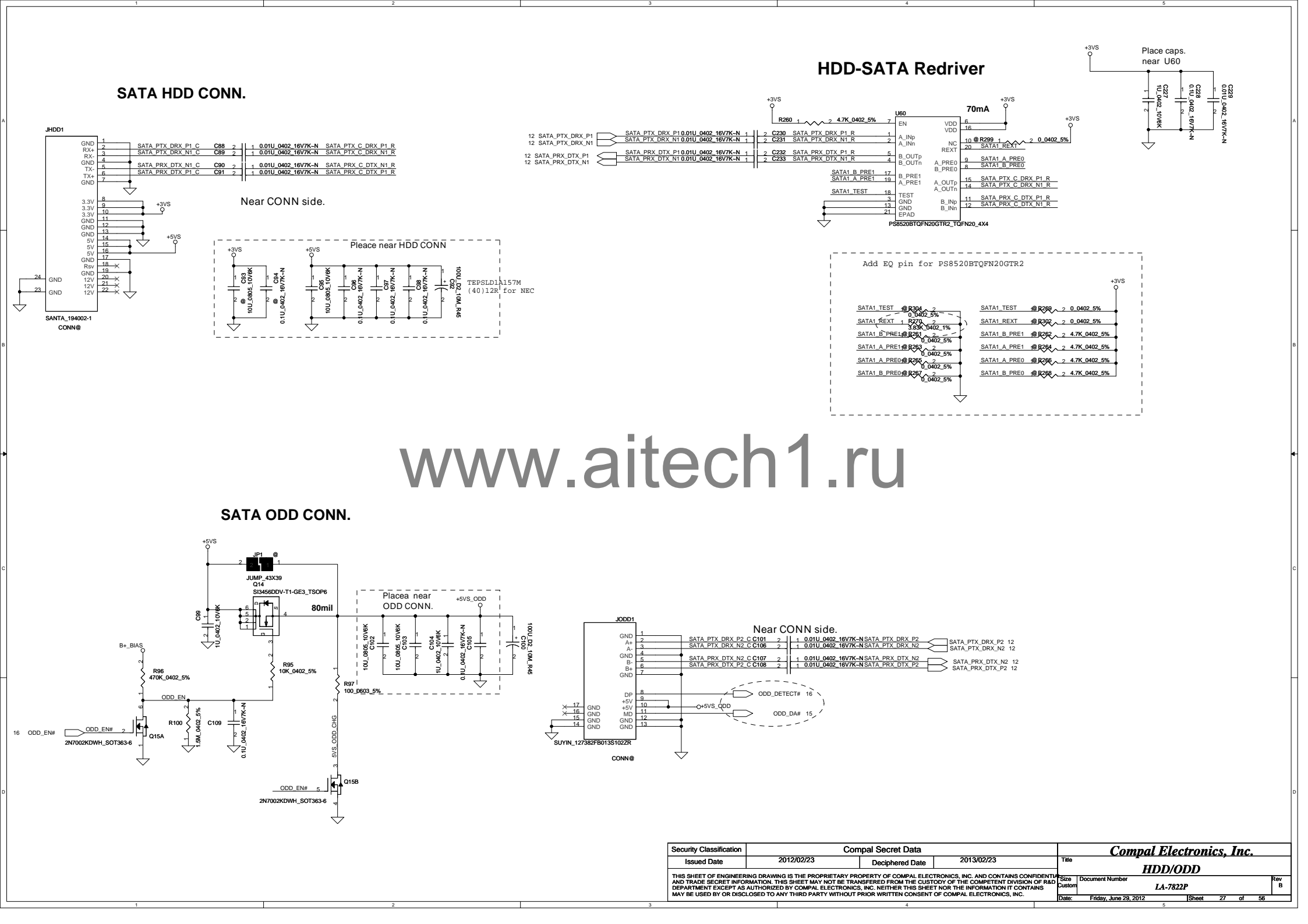
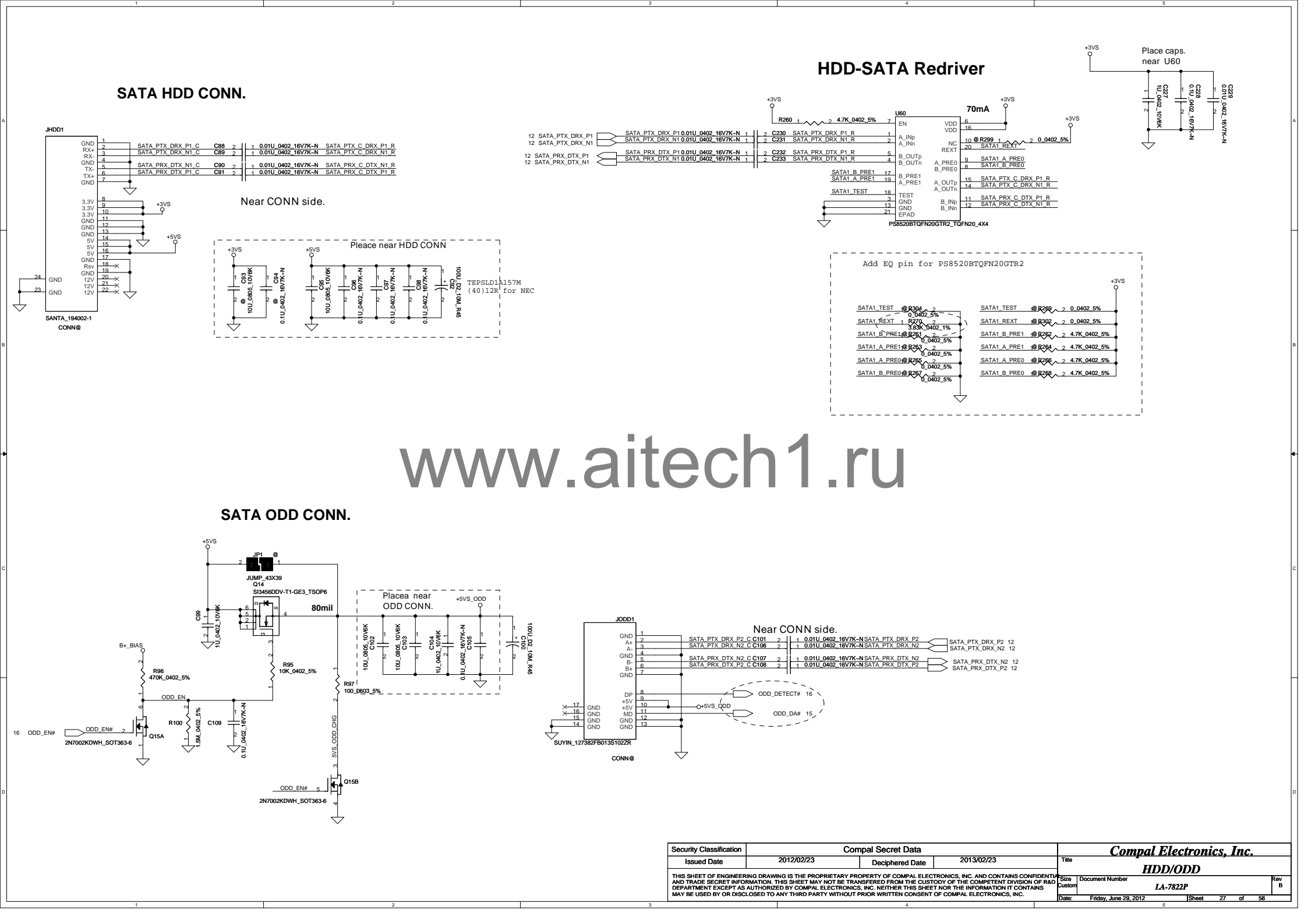
Near CONN side.

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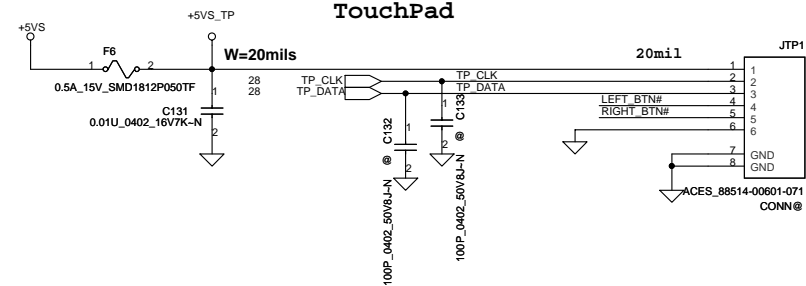
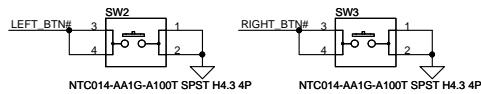
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Issued Date	2012/02/23	Deciphered Date	2013/02/23	Title	HDD/ODD
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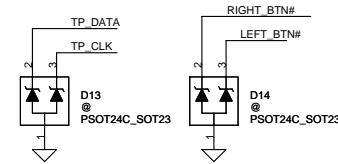
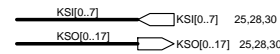
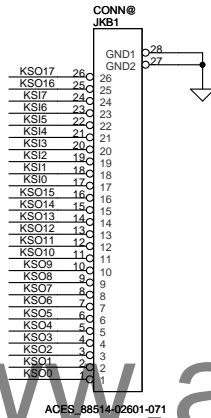
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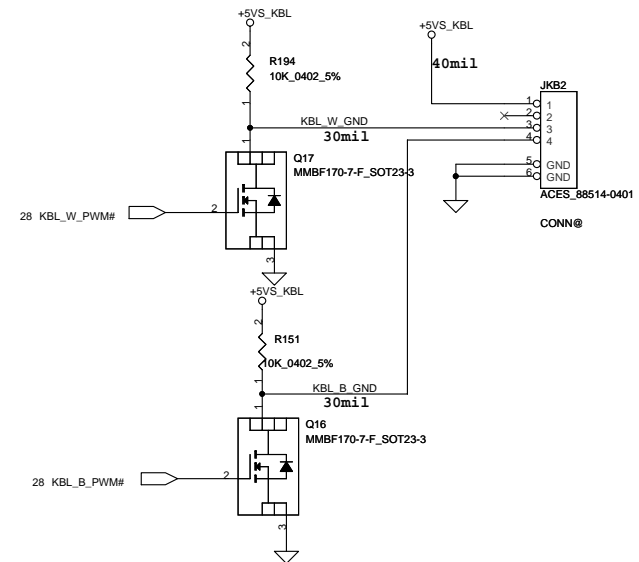
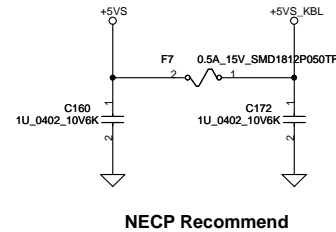
INT_KBD CONN.

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KSI3	C136	100P_0402_50V8J-N	KSI6	C137	100P_0402_50V8J-N
KSO9	C138	100P_0402_50V8J-N	KSI5	C139	100P_0402_50V8J-N
KSI2	C140	100P_0402_50V8J-N	KSO0	C141	100P_0402_50V8J-N
KSI1	C142	100P_0402_50V8J-N	KSO1	C143	100P_0402_50V8J-N
KSO10	C144	100P_0402_50V8J-N	KSO2	C145	100P_0402_50V8J-N
KSO11	C146	100P_0402_50V8J-N	KSI4	C147	100P_0402_50V8J-N
KSI0	C148	100P_0402_50V8J-N	KSO3	C149	100P_0402_50V8J-N
KSO12	C150	100P_0402_50V8J-N	KSO4	C151	100P_0402_50V8J-N
KSO13	C152	100P_0402_50V8J-N	KSO6	C153	100P_0402_50V8J-N
KSO14	C154	100P_0402_50V8J-N	KSO6	C155	100P_0402_50V8J-N
KSO15	C156	100P_0402_50V8J-N	KSO7	C157	100P_0402_50V8J-N
KSO16	C158	100P_0402_50V8J-N	KSO17	C159	100P_0402_50V8J-N

Near JKB1



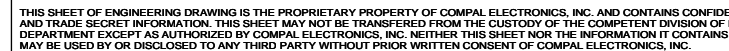
KB BackLight Control



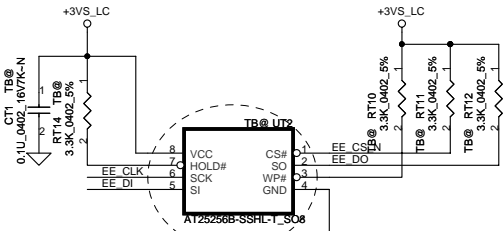
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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EC Beep



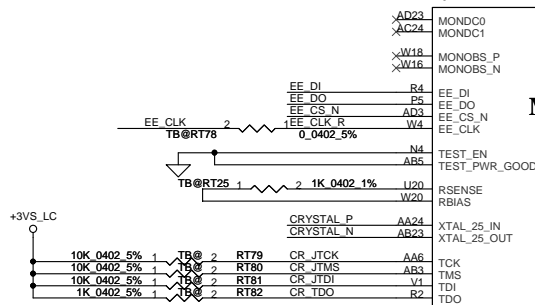
need to check connect to +3VS_LC or +3VS_POC



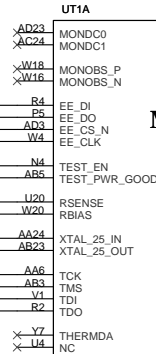
EEPROM

ATMEL:AT25256B, AT25512
CAT:CAT25256
ST:M95256-W6, M95512-W6
MICROCHIP:25AA256, 25LC256

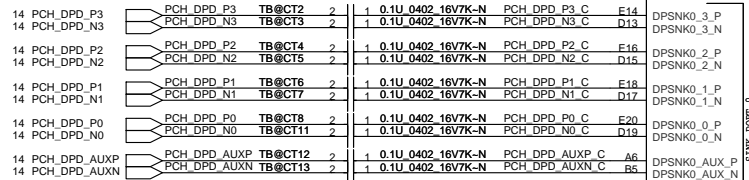
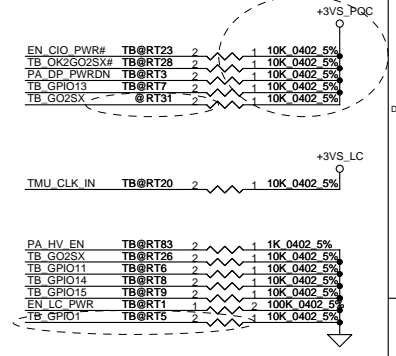
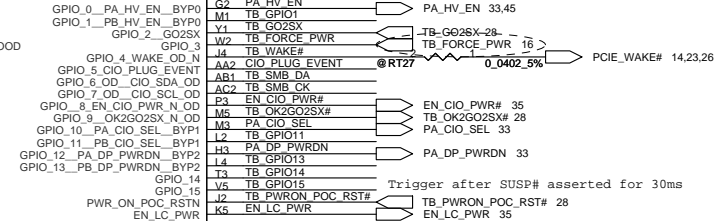
RT77 and CT120 close to UT2



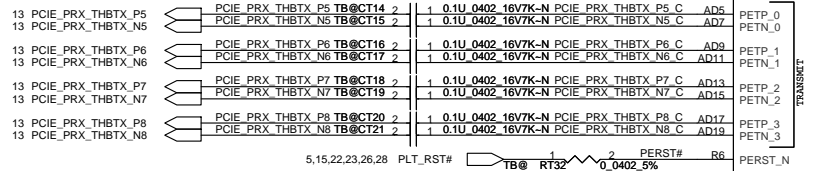
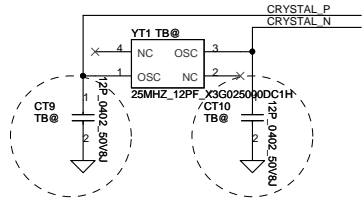
intra pair skew: 5 mil.
inter pair skew: 10 mil



MISC



TO PCH 14 DPD_HPD

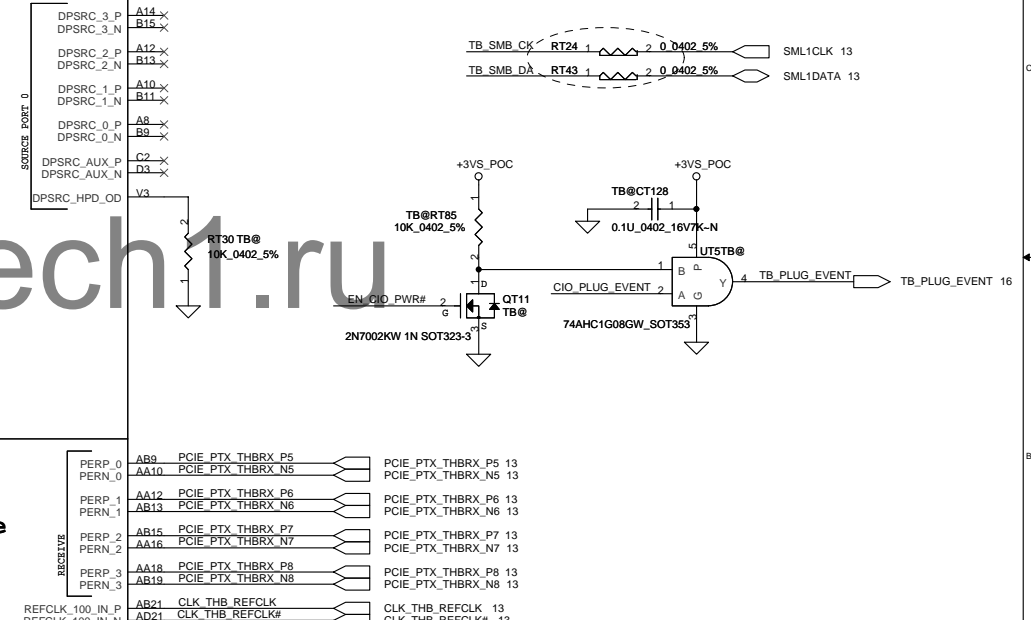


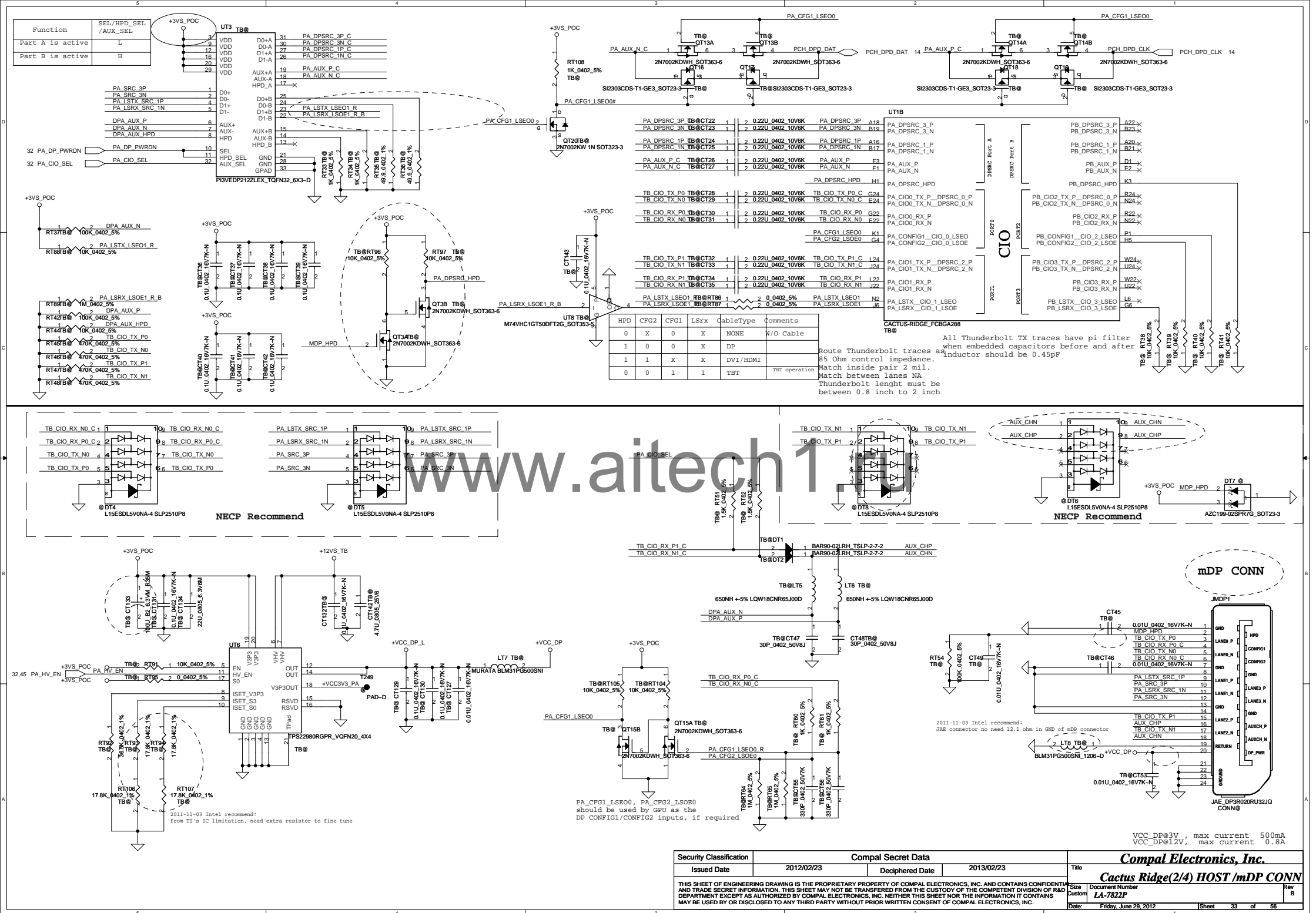
5,15,22,23,26,28 PLT_RST#

TB@ CACTUS-RIDGE_FCBGA288

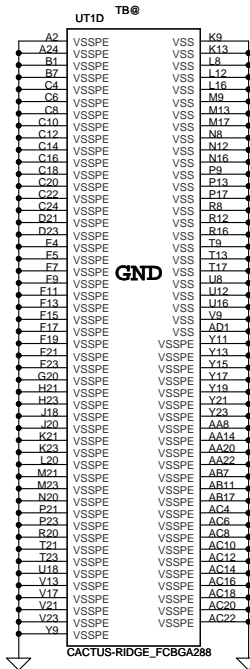
Display Port

PCIe



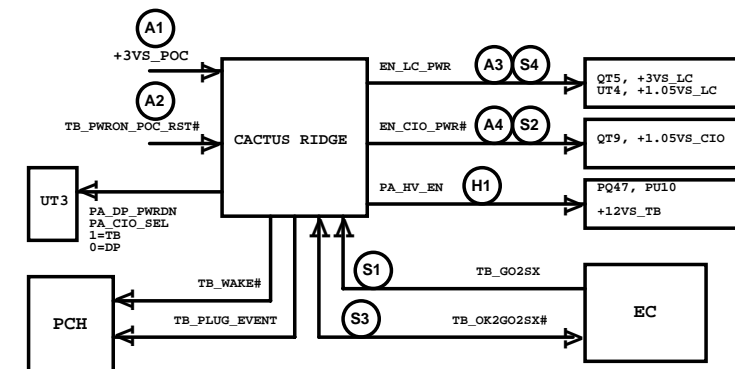
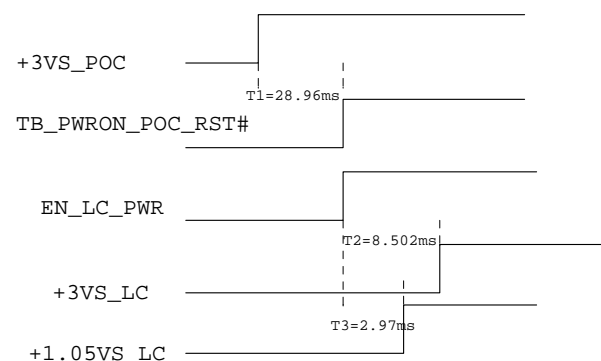
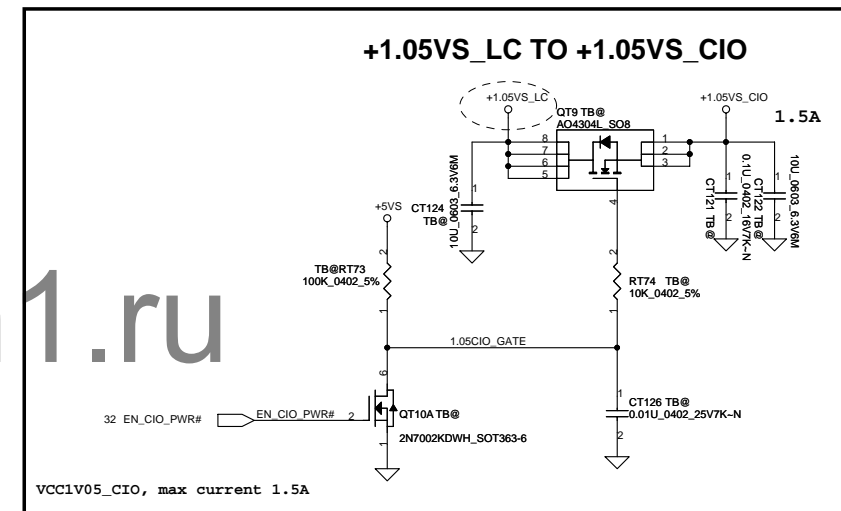
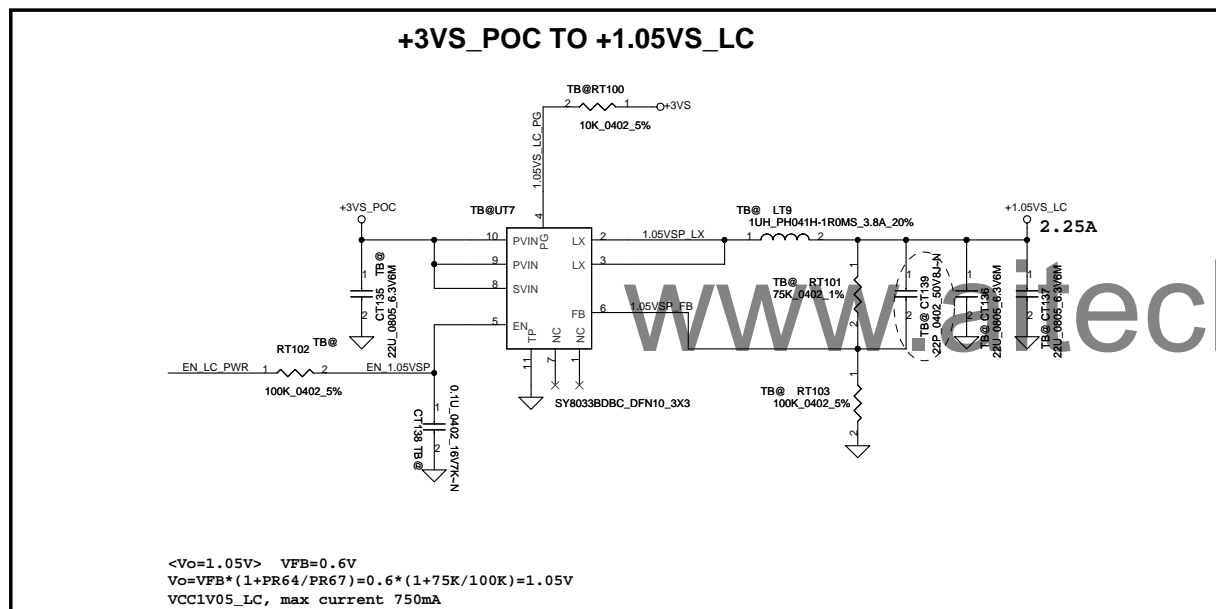
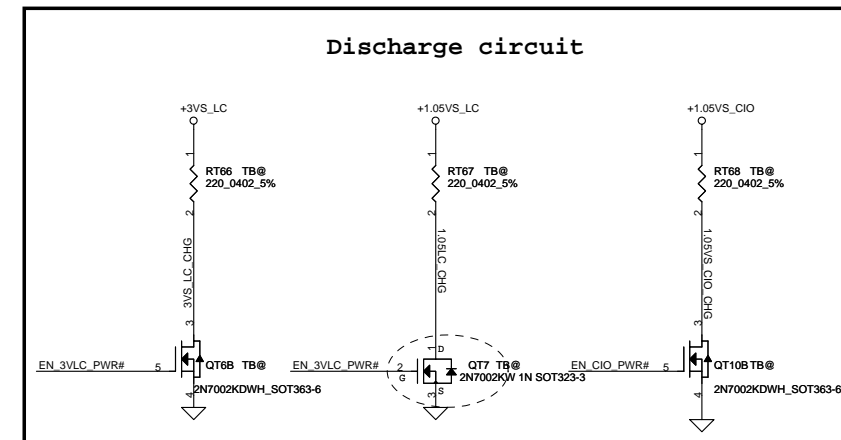
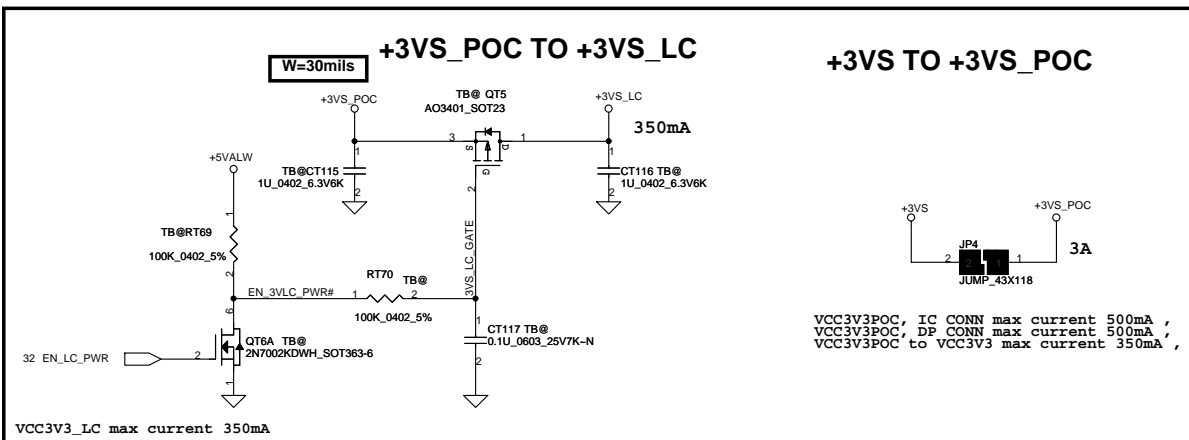


The schematic diagram illustrates the Cactus Ridge FCBGA288 board, showing the UT1C TB@ connector and various power and signal pins. The board includes a VCC section with pins for VCC1P0_ON, VCC1P0_PE, VCC1P0_DP, and VCC3P3. It also features a TB@ connector with pins for TB@ CT113, TB@ CT114, TB@ CT109, TB@ CT110, TB@ CT108, TB@ CT107, TB@ CT106, TB@ CT105, TB@ CT104, TB@ CT103, TB@ CT102, TB@ CT101, TB@ CT100, TB@ CT109, TB@ CT108, TB@ CT107, TB@ CT106, TB@ CT105, TB@ CT104, TB@ CT103, TB@ CT102, TB@ CT101, TB@ CT100. The board is powered by +1.05VS/LC and +3VS_POC.



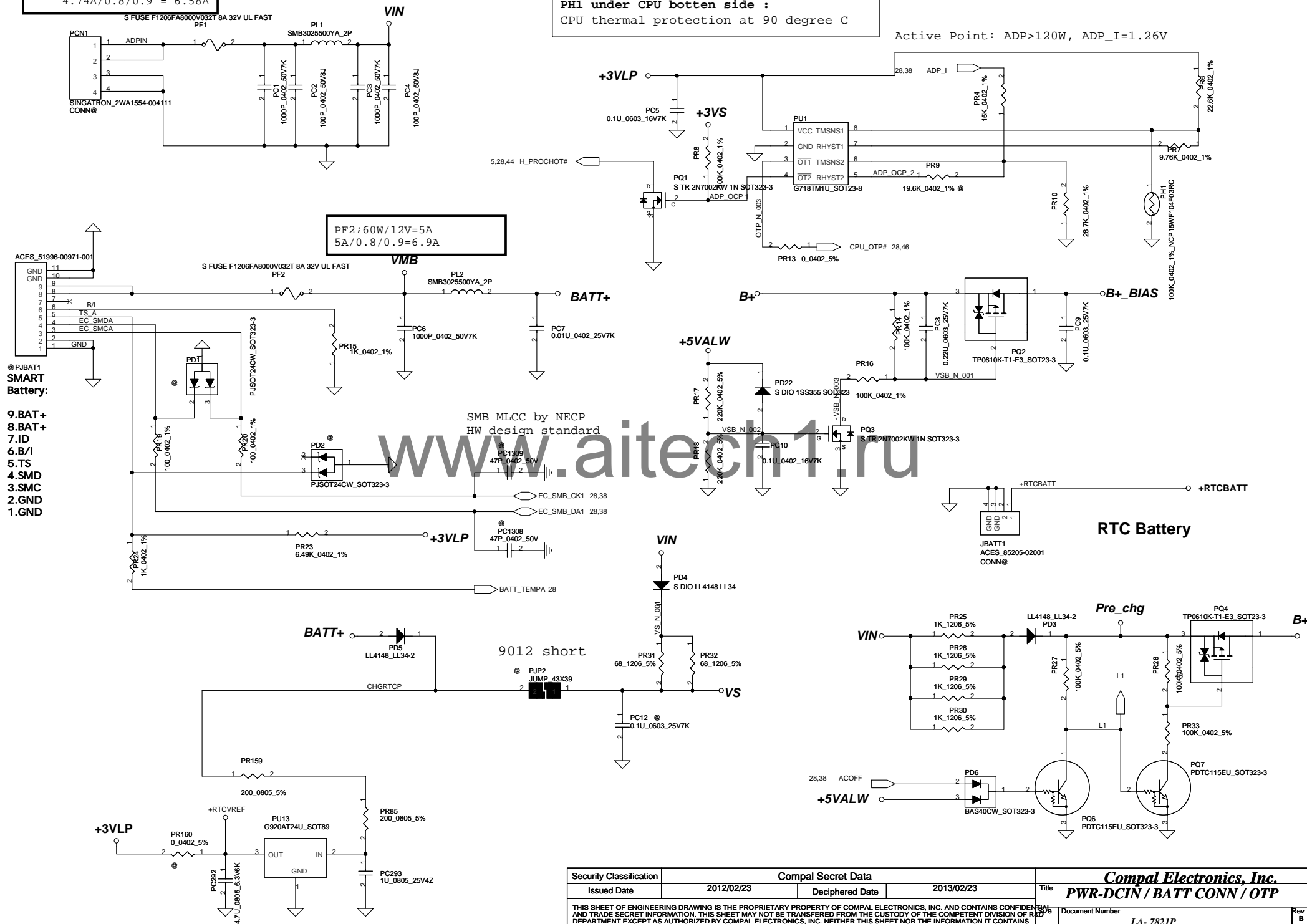
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										Customer		LA-7822P				B			
										Date:		Friday, June 29, 2012				Sheet		34 of 56	



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Active Point: ADP>120W, ADP_I=1.26V



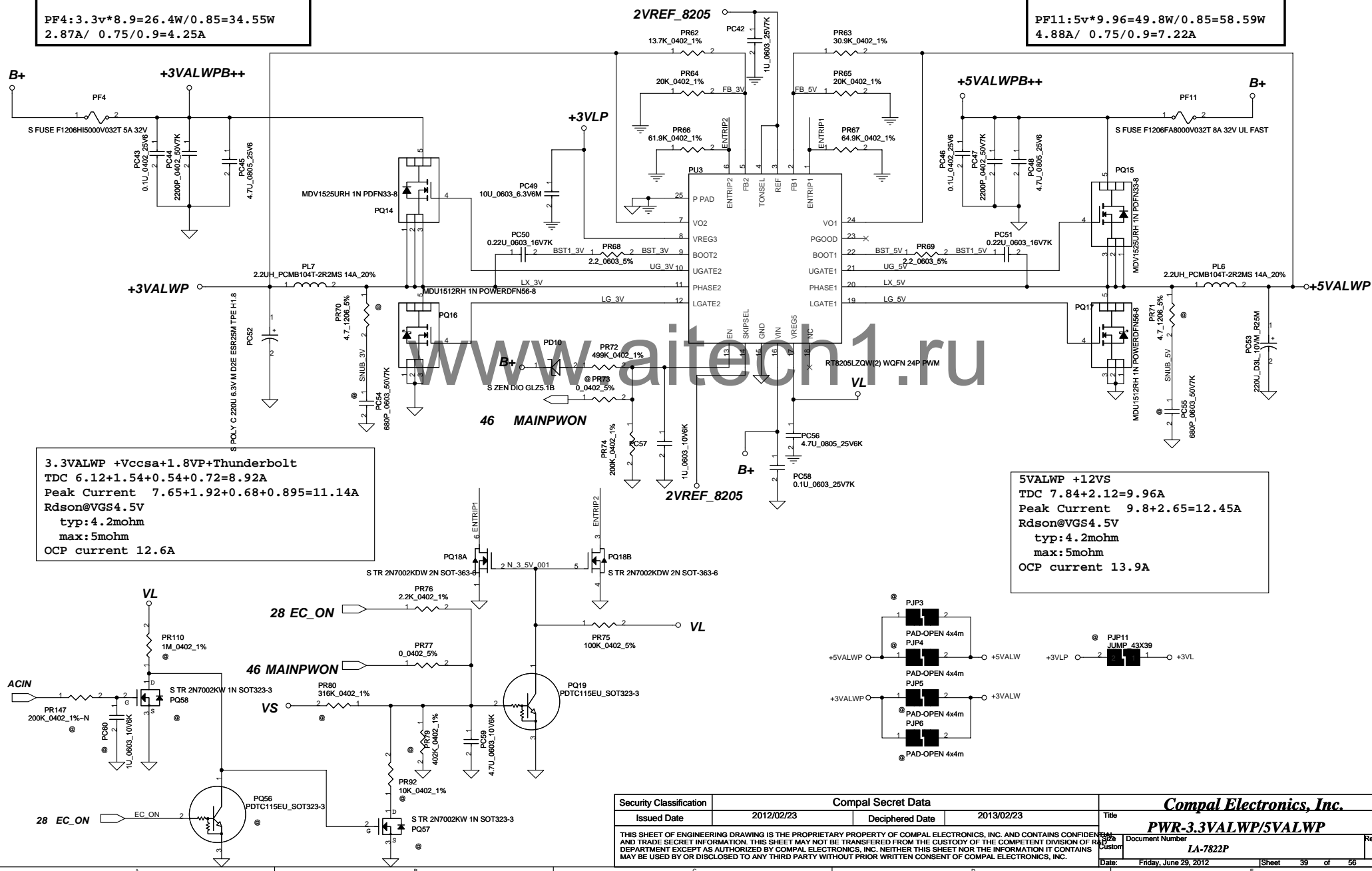
Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR-DCIN / BATT CONN / OTP	
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$$\text{PF4: } 3.3\text{v} \times 8.9 = 26.4\text{W} / 0.85 = 34.55\text{W}$$

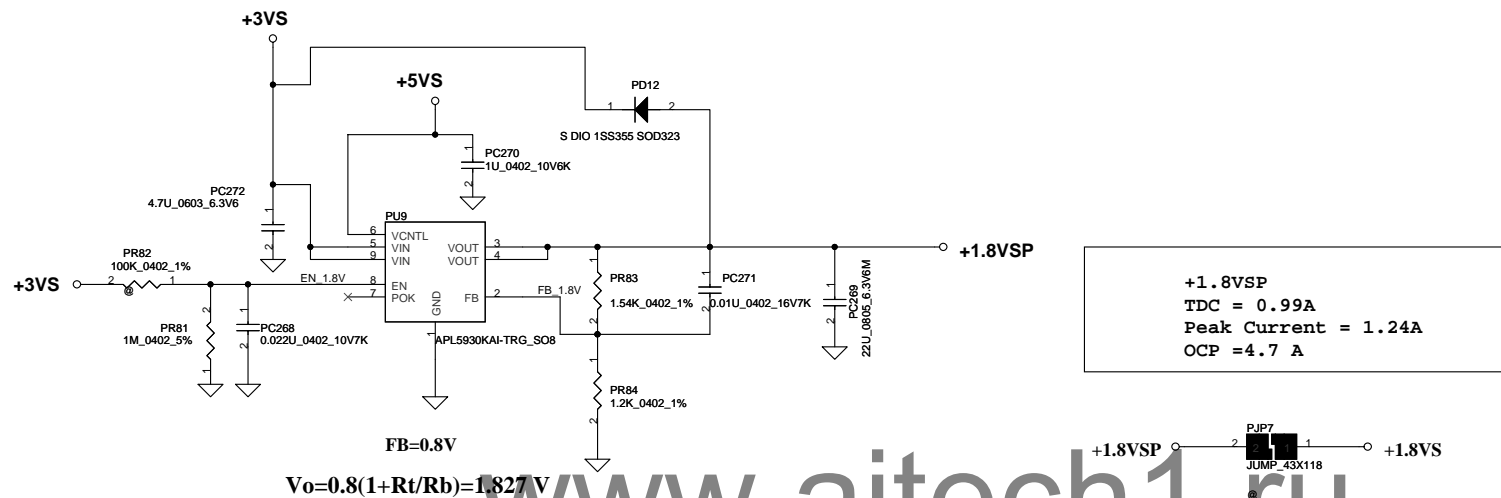
$$2.87\text{A} / 0.75 / 0.9 = 4.25\text{A}$$

$$\text{PF11: } 5\text{V} \times 9.96 = 49.8\text{W} / 0.85 = 58.59\text{W}$$

$$4.88\text{A} / 0.75 / 0.9 = 7.22\text{A}$$



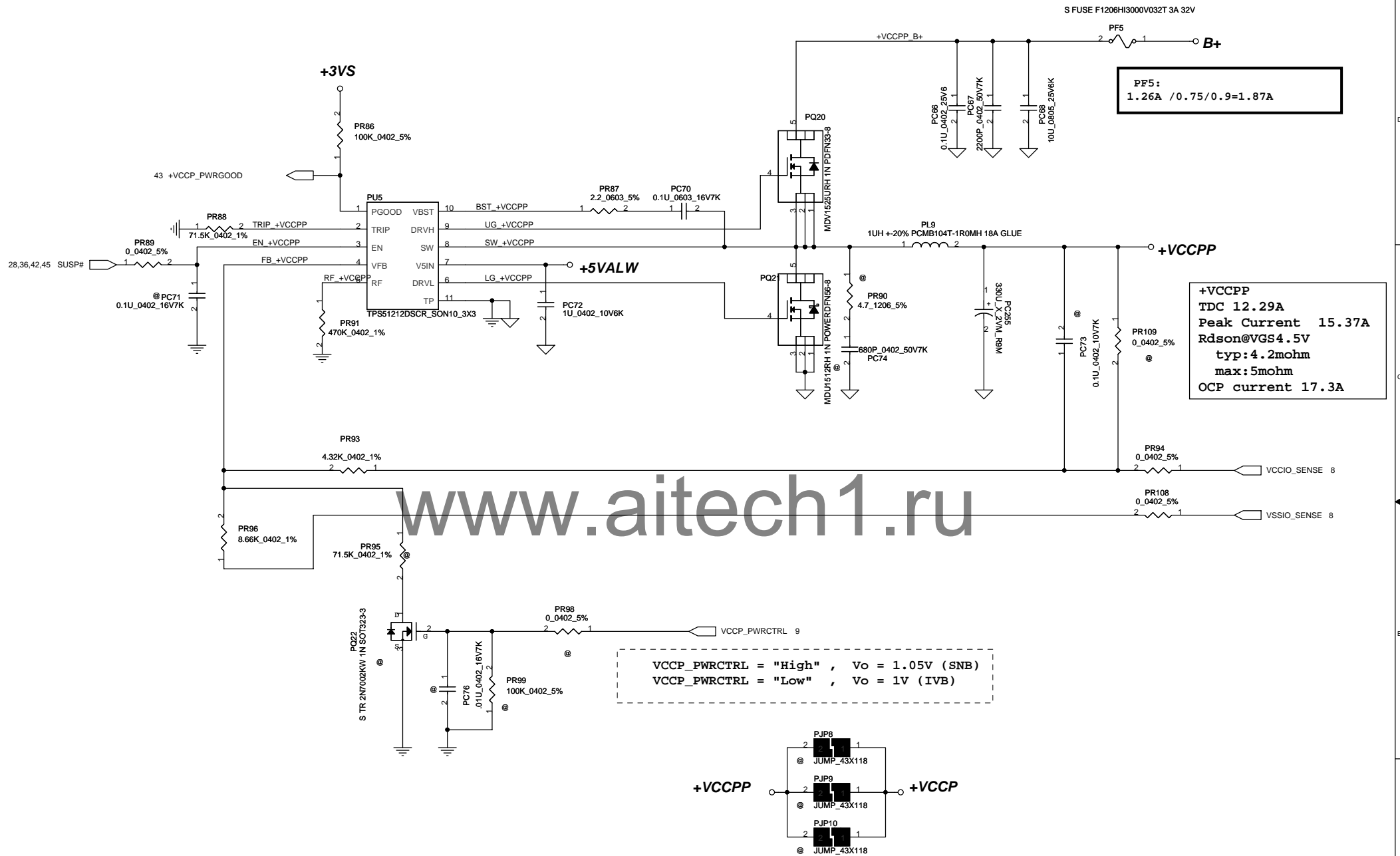
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Issued Date	2012/02/23	Deciphered Date	2013/02/23	Title	PWR-3.3VALWP/5VALWP
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$$V_o = 0.8(1 + R_t/R_b) = 1.827 \text{ V}$$

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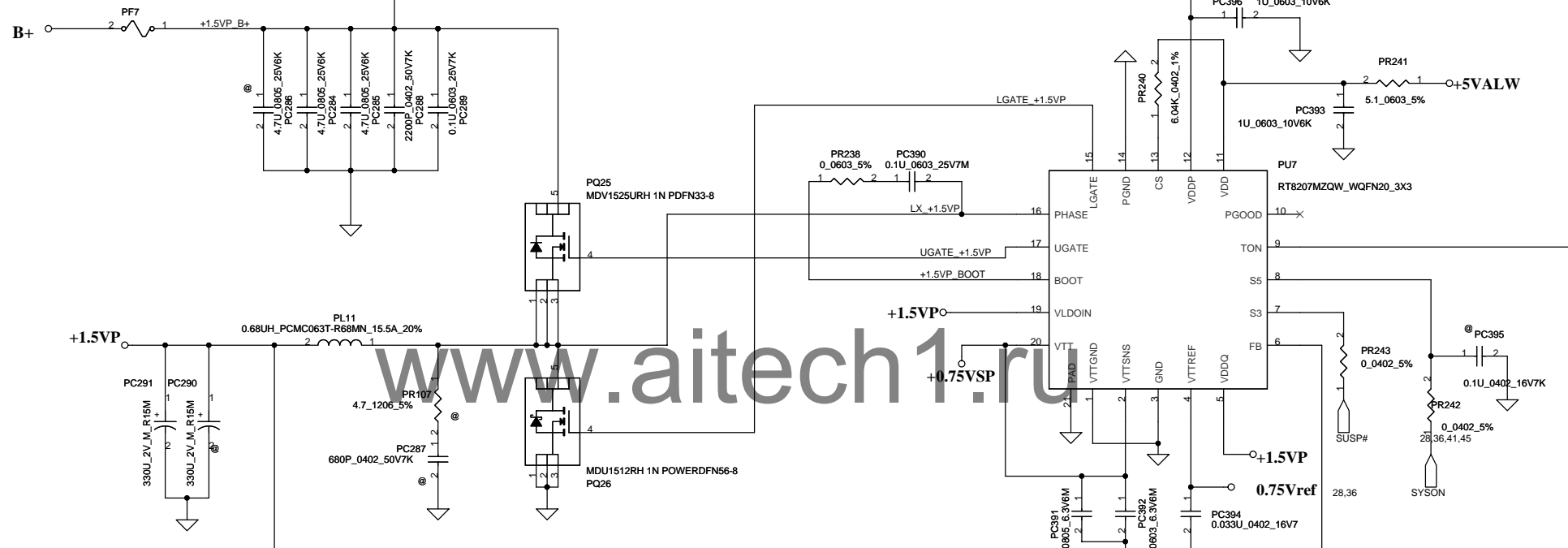


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$$PF7: 0.75V \times 1.2 + 1.5V \times 8.92 = 14.28W / 0.85 = 16.8$$

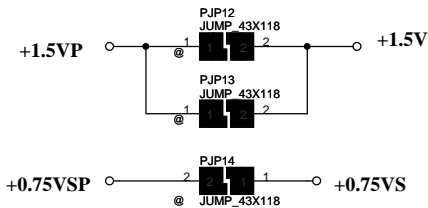
$$1.4A / 0.75 / 0.9 = 2.07A$$

S FUSE F1206HI3000V032T 3A 32V



+1.5VP
 TDC Current = 8.92A
 Peak Current = 11.15A
 OCP current = 13.5A
 Rdson@VGS4.5V
 typ:4.2mohm
 max:5mohm

+0.75VSP
 TDC = 1.2A
 Peak Current = 1.5A
 OCP fixed to 1.6A



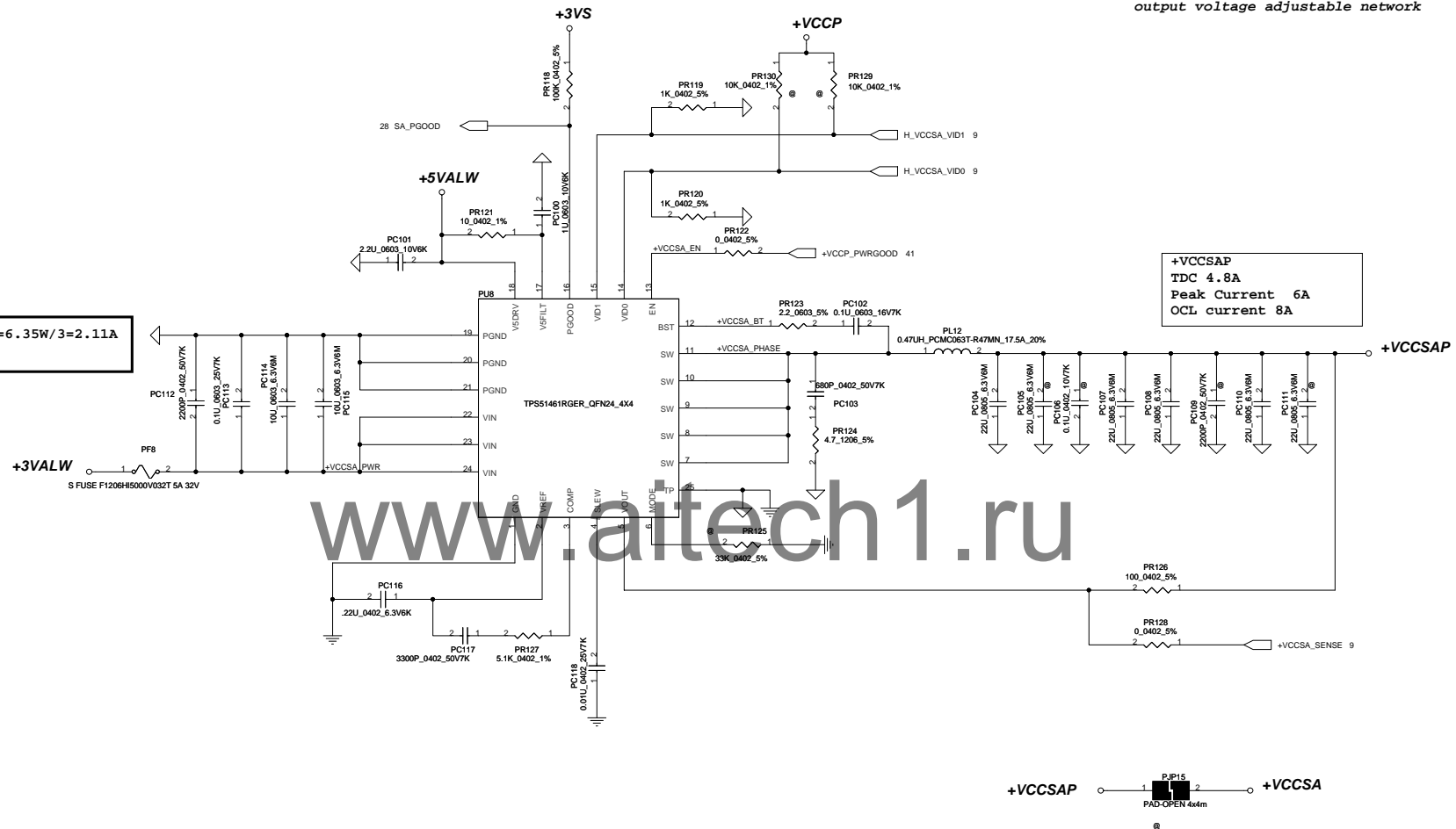
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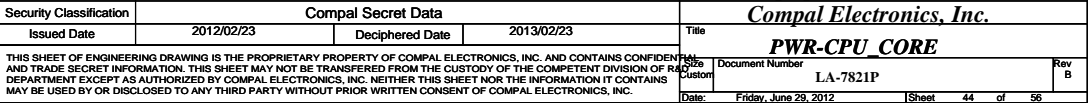
The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

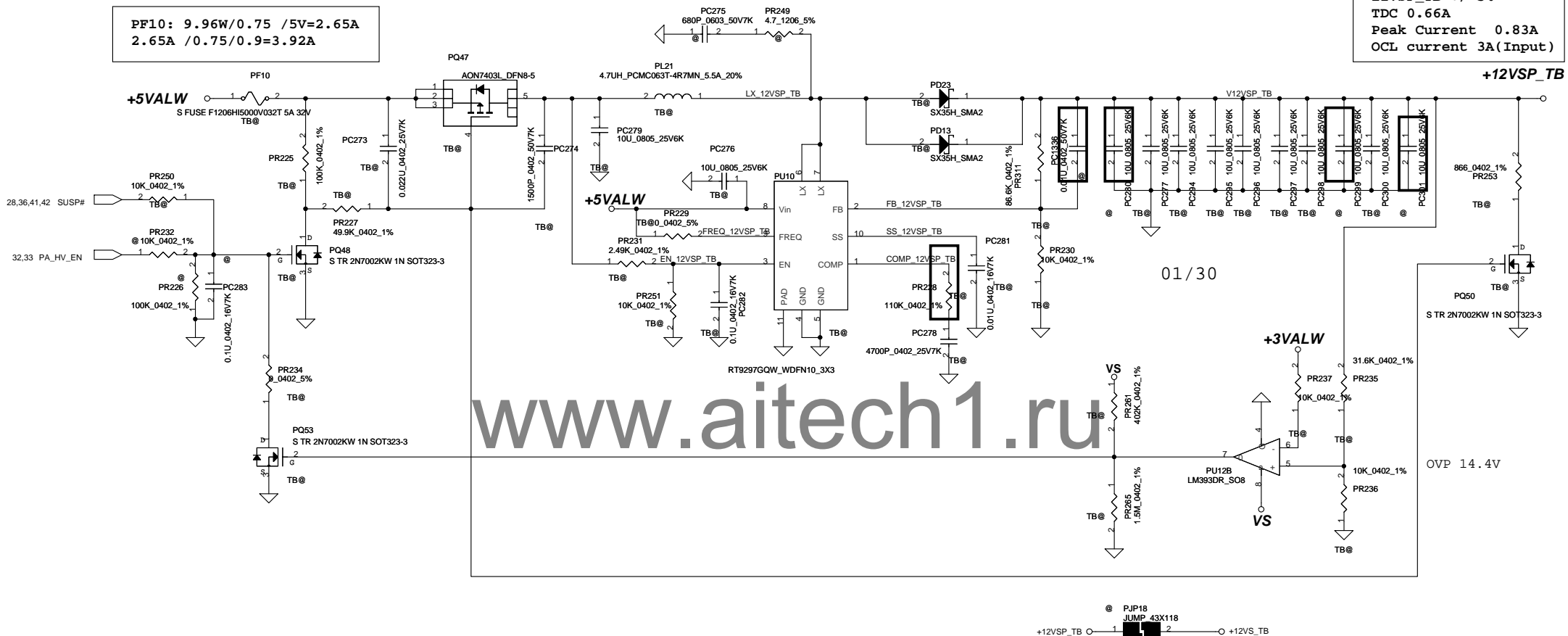
$PF8: 0.9V \cdot 6A = 5.4 / 0.85 = 6.35W / 3 = 2.11A$
 $2.11A / 0.75 / 0.88 = 3.2A$





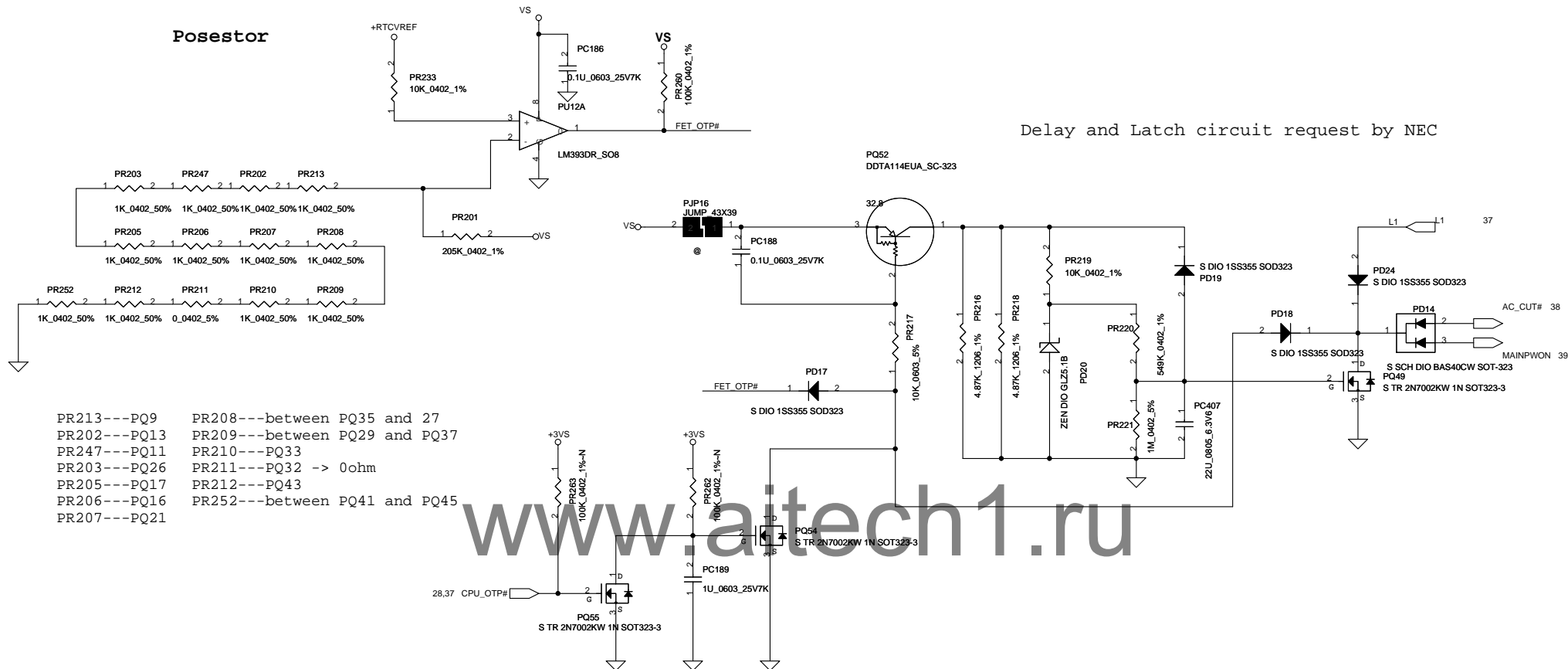
PF10: 9.96W/0.75 /5V=2.65A
2.65A /0.75/0.9=3.92A

12VSP_TB +/-5%
TDC 0.66A
Peak Current 0.83A
OCL current 3A(Input)



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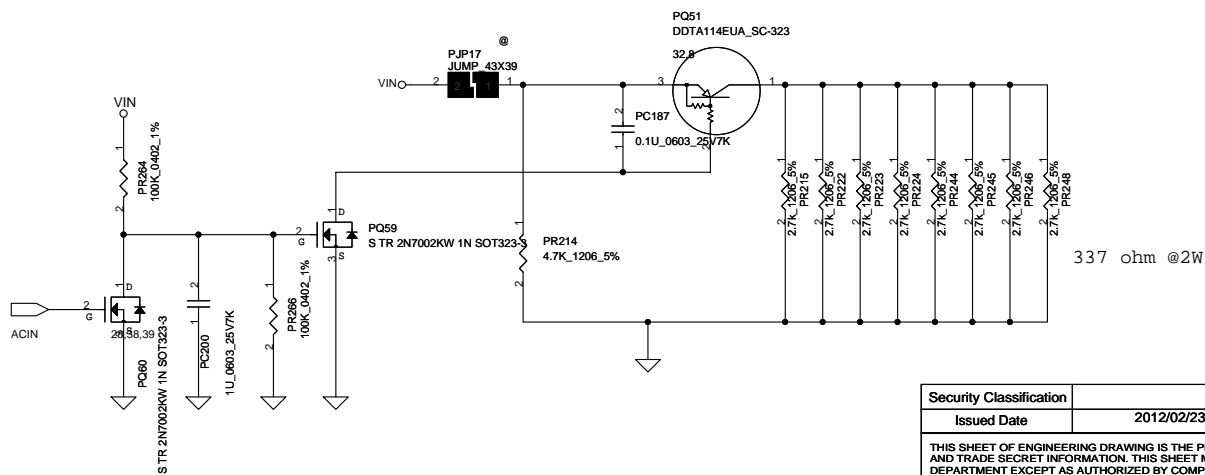
Posestor



Delay and Latch circuit request by NEC

PR213---PQ9
PR202---PQ13
PR247---PQ11
PR203---PQ26
PR205---PQ17
PR206---PQ16
PR207---PQ21
PR208---between PQ35 and 27
PR209---between PQ29 and PQ37
PR210---PQ33
PR211---PQ32 -> 0ohm
PR212---PQ43
PR252---between PQ41 and PQ45

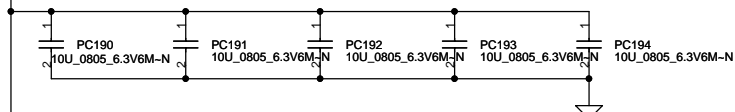
Remaining voltage discharge circuit request by NEC



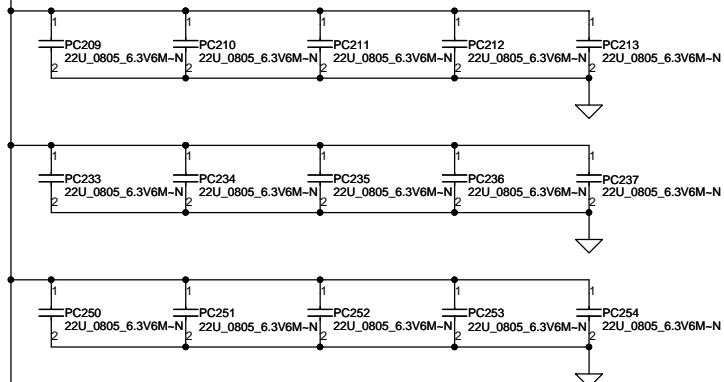
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Issued Date	2012/02/23	Deciphered Date	2013/02/23	Compal Electronics, Inc.	
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+VCC_CORE

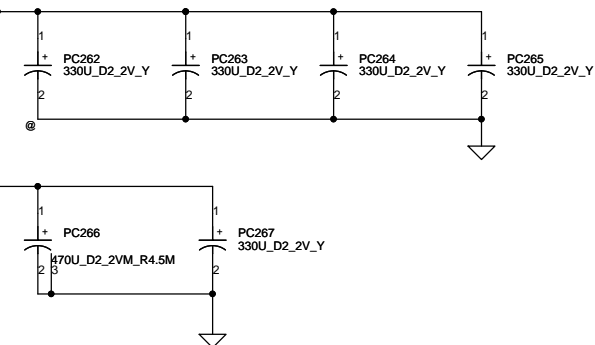
+VCC_CORE



+VCC_CORE

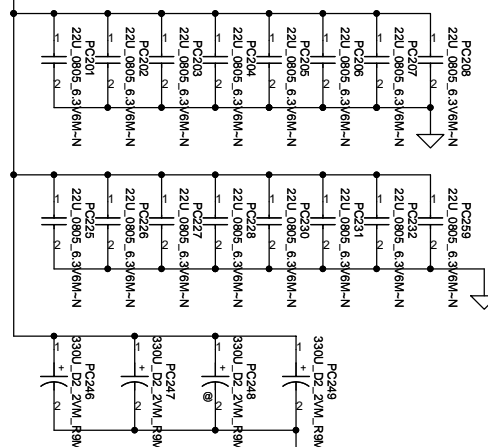


+VCC_CORE



+VCC GFXCORE_AXG

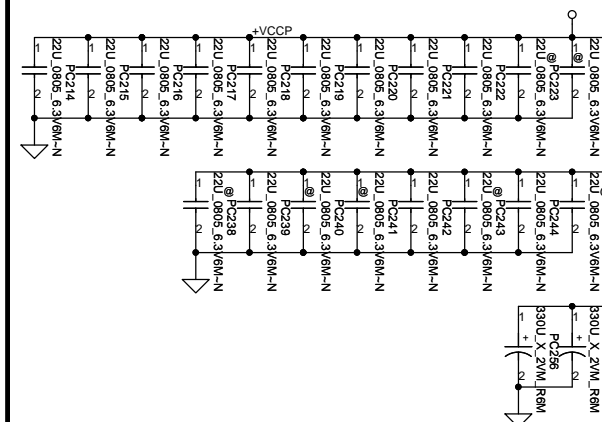
+VCC GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+VCCP



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Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DCIN / BATT CONN	11' 08/23	Compal_Aaron	remove PR11,PR21		
2	44	CPU_VORE	11' 08/23	Compal_Aaron	change LS MOS	Change (SB00000P300 S TR AON5788 1N DFN) to (SB00000SY00 S TR MDU1512RH 1N POWERDFN56-8) Location :PQ27,28,31,32,35,36,39,40,43,44	
3	44	CPU_CORE	11' 08/23	Compal_Aaron	change HS MOS	Change (SB00000NW00 S TR AON6414AL 1N DFN) to (SB00000S600 S TR MDV1525URH 1N PDFN33-8) Location :PQ29,33,37,39,41,45	
4	42	1.05VSP	11' 08/23	Compal_Aaron	adjust OCP	Change (SD034374280 S RES 1/16W 37.4K +-1% 0402) to (SD034100380 RES 1/16W 100K +-1% 0402) Location :PR101	
5	39	3.3VALWP/5VALWP	11' 08/23	Compal_Aaron	adjust OCP	Change (SD034140380 S RES 1/16W 140K +-1% 0402) to (SD034154380 S RES 1/16W 154K +-1% 0402) Location :PR66	
6	40	1.8VSP	11' 08/23	Compal_Aaron	for current limit	Change (SD028000080 S RES 1/16W 0 +-1% 0402) to (SD034100280 RES 1/16W 10K +-1% 0402) Location :PR82	
7	39	3.3VALWP/5VALWP	11' 08/23	Compal_Aaron	adjust OCP	Change (SD034178380 RES 1/16W 178K +-1% 0402) to (SD034200380 RES 1/16W 200K +-1% 0402) Location :PR67	
8	44	CPU_CORE	11' 08/26	Compal_Aaron	add PF6	add PF6	
9	38	CHARGER	11' 08/29	Compal_Aaron	solve can not power on issue	connect PR1313 pin 2 from P3 to VIN	
10	46	PROSESTOR	11' 08/29	Compal_Aaron	solve can not power on issue	connect PR262 pin 1 from VIN to 3VS	
11	37	CHARGER	11' 08/29	Compal_Aaron	adjust snubber	change PC37 form 1000pF to 680pF	
12	43	VCCSAP	11' 08/29	Compal_Aaron	adjust snubber	change PC103 form 1000pF to 680pF	
13	41	VCCP	11' 08/29	Compal_Aaron	adjust snubber	change PC74 form 1000pF to 680pF	
14	44	CPU_CORE	11' 08/29	Compal_Aaron	for current rating	change PF9 form 5A to 8A	
15	45	12VSP_TB	11' 08/29	Compal_Aaron	for current rating	change PF11 form Little to AEM	
16	44	CPU_CORE	11' 08/29	Compal_Aaron	adjust AXG OCP	change PR713 from 412 ro 442 ohm	
17	39	3.3VALWP/5VALWP	11' 08/29	Compal_Aaron	adjust OCP	Change PR66 form 154k to 174k	
18	39	3.3VALWP/5VALWP	11' 08/29	Compal_Aaron	adjust OCP	Change PR67 form 200k to 182k	
19	38	CHARGER	11' 08/31	Compal_Aaron	for protection	add PD28	

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
20	45	12VSP-TB	11' 08/31	Compal_Aaron	add 0.01uF for transient	add PC1336	
21	46	PROSESTOR	11' 08/31	Compal_Aaron	add PR248	add PR248	
22	38	CHARGER	11' 09/01	Compal_Aaron	by FAE review	change PR1331 10ohm to 0ohm	
23	38	CHARGER	11' 09/01	Compal_Aaron	for current limit	add PR1332	
24	45	12VSP_TB	11' 09/01	Compal_Aaron	for power sequence	connect PR231 pin 1 to PQ47 pin5	
25	38	CHARGER	11' 09/01	Compal_Aaron	add 0 ohm	add PR1333	
26	45	12VSP_TB	11' 09/02	Compal_Aaron	add 10kohm	add PR250	
27	38	CHARGER	11' 09/02	Compal_Aaron	change CHG IC to BQ24737	add CHG circuit	
28	39	3.3VALWP/5VALWP	11' 09/03	Compal_Aaron	adjust ocp	change PR66 to 61.9k	
29	39	3.3VALWP/5VALWP	11' 09/03	Compal_Aaron	adjust ocp	change PR67 to 64.9k	
30	39	3.3VALWP/5VALWP	11' 09/03	Compal_Aaron	for current design	change PL7 form SH000000IC00 3.3uH to SH000000O600 2.2uH	
31	42	1.5VSP	11' 09/03	Compal_Aaron	adjust ocp	change PR240 to 6.04k	
32	41	VCCPP	11' 09/03	Compal_Aaron	adjust ocp	change PR88 to 71.5k	
33	38	CHARGER	11' 09/03	Compal_Aaron	CHARGER Solution	change CHG circuit form ISL88731C to BQ24737	
34	38	CHARGER	11' 09/03	Compal_Aaron	for current design	change PL4 form 10uH to 4.7uH	
35	45	12VSP_TB	11' 09/06	Compal_Aaron	for EN pin	add PR251 10kohm	
36	38	CHARGER	11' 09/06	Compal_Aaron	change net	change BQ24737_VDD from PD31 pin1 to PC317 pin2	
37	47	PROSESTOR	11' 09/08	Compal_Aaron	add prosestor by NEC	add PR252	
38	47	PROSESTOR	11' 11/01	Compal_Aaron	for Overshoot	add PR265, PR266	

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39	40	1.8VSP	11' 11/01	Compal_Aaron	for power sequency	change PU9 EN form SUSP# to 3VS	
40	44	CPU / AXG	11' 11/01	Compal_Aaron	adjust transient	change PR261 form 100kohm to 402kohm	
41	44	CPU / AXG	11' 11/01	Compal_Aaron	adjust transient	change PR313 form 432kohm to 412kohm	
42	44	CPU / AXG	11' 11/01	Compal_Aaron	adjust over shoot	change PL16,17,18 form 0.36uH to 0.22uH	
43	38	CHARGER	11' 11/01	Compal_Aaron	adjust current limit	change PR321 form 750k to 549k ohm	
44	38	CHARGER	11' 11/01	Compal_Aaron	adjust current limit	change PR324 form 95.3k to 100k ohm	
45	47	PROCESSOR DECOUPLING	11' 11/03	Compal_Aaron	for AXG ripple	add PC230, PC231, PC 232, PC259	
46	44	CPU / AXG	11' 11/03	Compal_Aaron	remove MOS	remove PQ30 PQ34 PQ38 PQ46 PQ42	
47	38	CHARGER	11' 11/03	Compal_Aaron	adapter change to 90W	change PF1 form 12A to 8A	
48	37	DCIN / BATT / OTP	11' 12/07	Compal_Aaron	adjust ADP protection >120W	change PR4 form 27.4K to 15K ohm	
49	38	CHARGER	11' 12/07	Compal_Aaron	for I_dischg current to 4A	change PR324 form 100k to 178k ohm	
50	38	CHARGER	11' 12/07	Compal_Aaron	for I_dischg current to 4A	change PR329 form 215k to 118k ohm	
51	42	1.5VSP	11' 12/07	Compal_Aaron	for dynamic voltage (IDLE test)	pop PR270, PR271	
52	42	1.5VSP	11' 12/07	Compal_Aaron	for dynamic voltage (IDLE test)	depop PR97	
52	45	12VSP_TB	11' 12/07	Compal_Aaron	for discharge circuit	change PR227 from 100k to 49.9k ohm	
53	39	5VALWP/ 3VALWP	11' 12/16	Compal_Aaron	for KB9012	change PR76 from 10k to 2.2k ohm	
54	40	1.8VSP	11' 12/19	Compal_Aaron	for power sequency	unmount PR82	
55	40	1.8VSP	11' 12/19	Compal_Aaron	for power sequency	change PC268 from 0.22uF to 0.022uF	
56	40	1.8VSP	11' 12/19	Compal_Aaron	for power sequency	change PR81 from 4.7k to 1M ohm	

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57	37	DCIN / BATT / OTP	11' 12/19	Compal_Aaron	change 90W BATT to 60W	change PF2 form 12A to 8A	
58	45	12VSP_TB	11' 12/19	Compal_Aaron	add capacitors	add PC302-309, PC311, PC312	
59	45	12VSP_TB	11' 12/20	Compal_Aaron	add capacitors	add PC723,PC724	
59	45	12VSP_TB	11' 12/20	Compal_Aaron	add discharge R	add PR253	
60	45	12VSP_TB	11' 12/20	Compal_Aaron	for discharge MOS	change PQ50 MOS A04466 to 2N7002	
61	44	VCORE / AXG	11' 12/22	Compal_Aaron	for thermal	add MOS PQ30,PQ34,PQ38	
62	45	12VSP_TB	11' 12/22	Compal_Aaron	by NEC request	change PR253 from 200k to 866 ohm	
63	44	VCORE / AXG	12' 01/02	Compal_Aaron	for TP thermal	mount MOS PQ30,PQ34,PQ38 to AON6428L	
64	44	VCORE / AXG	12' 01/02	Compal_Aaron	for TP thermal	unmount MOS PQ29,PQ33,PQ37	
65	44	VCORE / AXG	12' 01/02	Compal_Aaron	for MOS quality	change MOS PQ41,PQ45 from AON6514 to AON6428L	
66	45	12VSP_TB	12' 01/30	Compal_Aaron	remove capacitors	delete PC302-309, PC311, PC312, PC723, PC724	
67	45	12VSP_TB	12' 01/30	Compal_Aaron	for dynamic test	unmount PC1336, PC280 ,PC299 ,PC301	
68	45	12VSP_TB	12' 01/30	Compal_Aaron	for dynamic test	change PR228 from 10k to 110k	
69	44	VCORE / AXG	12' 02/08	Compal_Aaron	for VCORE OCP	change PR759 from 430 to 442 ohm	
70				Compal_Aaron			
71				Compal_Aaron			
72				Compal_Aaron			
73				Compal_Aaron			
74				Compal_Aaron			

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1		HW Design	0.01	20	Modify JLCD1 NET	08/22	
2		HW Design	0.01	09,35,36	Change AO4430L to AO4304L location:QC3 QT9 U14 U15	08/22	
3		HW Design	0.01	27,36	Change SI3456BDV to SI3456DDV location:Q14 Q25 Q26	08/22	
4		HW Design	0.01	27,36	Change SI3456BDV to SI3456DDV location:Q14 Q25 Q26	08/22	
5		NECP Recommend	0.01	29	Change JTP1 to 12PIN	08/23	
6		NECP Recommend	0.01	26	Remove WLAN JMINI1 +1.5VS	08/23	
7		HW Design	0.01	34	Change CT113 CT114 CT60 CT78 to 1U	08/23	
8		ME Recommend	0.02	34	SWAP JTP1 Pin define	08/28	
9		ME Recommend	0.02	20	Update JLCD1 and JCM1 footprint	08/29	
10		ME Recommend	0.02	24	Update JHP1 and JM1C1 footprint	08/29	
11		NECP Recommend	0.02	28,23,26 14,30	Add 0.1U in U9,U57,U61,UH5,U58,U59	08/30	
12		NECP Recommend	0.02	22	R44 change to un mount	08/30	
13		NECP Recommend	0.02	26	Mount R114	08/30	
14		NECP Recommend	0.03	26	Add Circuit for INTEL AOAC Fuction	08/31	
15		NECP Recommend	0.03	28	Add R295 R296 for INTEL AOAC Fuction	08/31	
16		HW Design	0.03	14	Add RH148 pull down Change R269 R290 pull high	09/01	
17		HW Design	0.03	33	Add JMDP1 footprint	09/01	
18		EC Recommend	0.03	12,28	Change net name ME_FLASH to ME_EN	09/01	
19		HW Design	0.03	15	Pull high GPIO2	09/01	
20		NECP Recommend	0.04	20	D1 Pin 6 connect to USB20_N4 D1 Pin 4 connect to USB20_P4	09/02	
21		NECP Recommend	0.04	29	Update JTP1 PIN Define	09/02	
22		NECP Recommend	0.04	12	Change RH2100 from 15ohm to 0ohm	09/02	
23		Power Design	0.04	28	mount C113 Add R297 for BST_CHARGE	09/02	
24		HW Design	0.04	16	Remove RH159 PCH Peci for Layout routing	09/02	
25		HW Design	0.05	26,27 30 23	Change R270, R292 to 2.61k Change R236, R249 to 2.61k Unmount R273,R277 Change R226 to 2.61k	09/06	
26		HW Design	0.05	32	Add CT140,CT141 close to UT1	09/07	

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1		HW Design	0.07	34 33	Change CT69,CT70,CT101 to 0.001U Change RT39 to 348K and RT94 to 35.7K	09/08	
2		HW Design	0.11	28	Change R210 to 220K	09/22	
3		HW Design	0.11	26 , 27	Change R270 and R292 to 3.83K	09/29	
4		HW Design	0.11	24	Change CA19 and CA21 footprint from 0805 to 0603	09/29	
5		HW Design	0.11	13 , 32	Change YH2 and YT1 from SJ100009B00 to SJ10000B700	09/30	
6		HW Design	0.11	9 , 17	Change CC135 ,CC161 ,CC162 ,CC163 ,CC164 ,CC165 ,CC166 ,CC168 ,CC169 ,CC170 ,CC171 ,CC173 ,CH30 ,CH44 footprint from 0805 to 0603	10/03	
7		HW Design	0.11	12	Change YH1 to FC-135 Change CH2 and CH3 to 15PF	10/04	
8		HW Design	0.11	5, 21, 23 25, 26, 32 35 , 36	Change SB0000096I0 to SB000009620 QC1,Q1,Q5,Q9,Q37,QT11,QT12,QT7,Q22,Q23,Q24,Q29,Q36	10/12	
9		HW Design	0.11	31, 36	Change Q27 from AO3413L to AO3419L Change Q21 from AO3413 to AO3419L	10/12	
10		HW Design	0.11	20	Change JCM1 to ACES_87213-1200G	10/18	
11		HW Design	0.11	25	Change JUSB3 to ACES_87036-1001-CP	10/18	
12		HW Design	0.11	15	Change RPH1 to RH32-RH36 Change RPH2 to RH37, RH39, RH41, RH50 Change RPH3 to RH159, RH184, RH185, RH186 Change RH187 to RH188, RH190, RH191, RH192 Remove RA31, RA32, RA33, RA34 Add LA6, LA7, LA8, LA9 Add CA26, CA27, CA28, CA30, CA32, CA33	10/19	
13		EMI Recommend	0.11	24	Change CC176 to 330U 6.3V M D2B ESR25M	10/20	
14		HW Design	0.11	09	Remove RCL30, RC129	10/24	
15		HW Design	0.11	05	Remove RC48	10/27	
16		HW Design	0.11	06	Remove RI05 RI25 RI26 RI27 RI42 RI43 RI44 RI45 U7	10/27	
17		HW Design	0.11	28	Remove C126 R147 C128 R128 R193 Add RI93, D27	10/27	
18		HW Design	0.11	30	Change D15 to YSCLAMP0524P_SLP2510P8-10-9	10/27	
19		HW Design	0.11	36	POP CI93 Q26 RI50 CI90 CI91 RI78 Q28 C915 RI53 POP Q27 CI92 RI79 Q36 R200 UNPOP RI75 RI76	10/27	
20		HW Design	0.11	28	Change R108 to 46.4K	10/27	
21		Intel Design	0.11	33	Add CT143, UT8 Add CT144, RT105, RT104	10/19	
22		HW Design	0.11	32	Change YT1 to X3G025000DC1H	10/19	
23		NECP Recommend	0.11	26 25	Add RI05 D17 Change Net USB20_N12 and USB20_P12 to JUSB3 Add Net RF_OFF# to JUSB3	10/28	
24		NECP Recommend	0.11	24	Pop CA44 10pF Change RA1654 to 33 ohm and RA1655 to 56ohm	10/28	
25		HW Design	0.11	25 28	Remove 930@ C126 D9 DI0 RI05 RI25 RI26 RI27 RI28 R142 R143 R144 R145 R193 U7	10/28	
26		NECP Recommend	0.12	25 26	Remove RI05 Change RF power from +5vs to +3vs	10/31	

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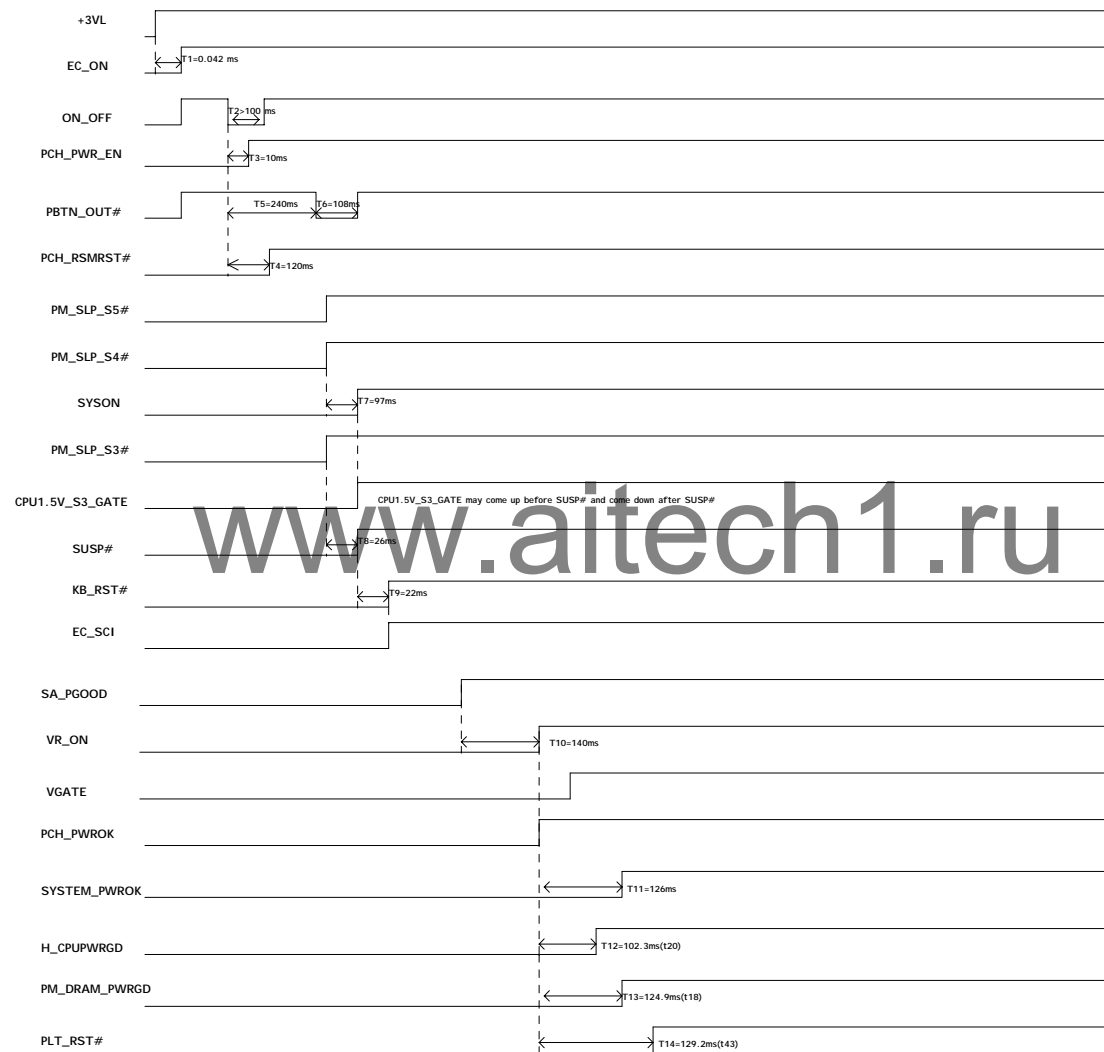
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.12	30	Add F10 C242 for USB3.0 Redriver Add R298 R193	10/31	
2		HW Design	0.12	26 27	Add R299 R302 Add R300 R301	11/01	
3		EMI Recommend	0.12	22	Change R46-R51 to 22ohm and C51 to 10pF	11/01	
4		EMI Recommend	0.12	30	Change D15 to AZ1045-04F DFN2510P10E ESD Add D27	11/01	
5		HW Design	0.12	29	Change SW2 and SW3 to NTC014-AA1G-A100T SPST H4.3 4P	11/01	
6		HW Design	0.12	17,36 27,30,24	Change CH36,C186,C189,C190,C193,C27,CA11,CA42,C162 Footprint from 0805 to 0603	11/01	
7		HW Design	0.12	21,23,25 36,26,05 35,32	Change Q1 Q5 Q9 Q22 Q23 Q24 Q29 Q36 Q37 QC1 QT7 QT11 QT12 to 2N7002KW 1N SOT323-3	11/01	
8		HW Design	0.12	29,36,24 25,27,18	Change C160, C172, C191, CA26, CA33, C66, C227, CH71 C104, C99 Footprint from 0603 to 0402	11/01	
9		HW Design	0.13	25	Add Q31 C207 R303 Q39 C208 R68	11/01	
10		HW Design	0.13	30	Modify netname LED_SRC to +LED_SRC Modify netname RE_PWR to +RE_PWR	11/02	
11		EMI Recommend	0.13	22	Delete Net SP14_MSClk_R	11/02	
12		Intel recommend	0.14	33	Delete RT98,RT99,RT55,RT58,RT59 Add RT106,RT107	11/03	
13		USB3.0 fine tune	0.14	23	Remove R281	11/03	
14		Thailand floods material issue	0.2	30	Change U10 to MAX14618ETA+T Change C161 to SANYO 150U 10V M D3L TPB LESR40M 2.8	11/09	
15		Thailand floods material issue	0.2	33	Change CT133 to SANYO 100U 6.3V M B2 LESR35M	11/09	
16		Thailand floods material issue	0.2	15,32	Change UH3 and UT5 74AHC1G08GW	11/09	
17		HW Design	0.21	15,32	Change H15 to 3P_1	12/01	
18		HW Design	0.21	26,27	Add R304 R305 for Pericom Repeater	12/01	
19		ME Recommend	0.21	25	Change JUSB3 to SP02000TR00(50224-01001-001)	12/01	
20		ME Recommend	0.21	20	Change JCM1 to ACES_50224-01001-001	12/01	
21		ME Recommend	0.21	33	Change UT8 to MC74VHC1GT50 Change RT93 RT94 RT106 RT107 to 17.8K Change EC PIN64 Net to PWR_WHITEBTN_LED#	12/01	
22		NECP Recommend	0.21	12 28	Add RH267 RH268 RH270 RH271 RH272 for LPC Add R115 R125 R113 R105 R101 for LPC	12/01	
23		NECP Recommend	0.21	25	Change R68 to 20K Change C208 to 0.1U	12/01	
24		NECP Recommend	0.21	16 26	Add C73 C126 Delete net BT_DIS#	12/01	
25		NECP Recommend	0.21	24	Change RA20 to 330K	12/01	
26		HW Design	0.21	30	Delete USB3.0 Redriver U58 U59 Add R205,R206,R208,R209 Add R213,R233,R214,R232	12/01	

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1		HW Design	0.21	12	Change CH2 CH3 to 18P	12/15	
2		HW Design	0.21	26 28	Add Net KILL_SWOFF# and Add R142 for WLAN Issue	12/15	
3		HW Design	0.21	36	Change C195 to 0.1U	12/18	
4		NECP Recommend	0.22	22	Add L11 for CardReader	12/18	
5		EMI Recommend	0.22	36	Add D6 FOR EMI	12/19	
6		HW Design	0.23	15 20 24	Change UH3 UV2 and UA5 to 74AHC1G08GW Change UA4 to M74VHC1GT125DF2G	12/20	
7		HW Design	0.21	36	Change UH4 to BD82HM77 QPRG C1 BGA 989P	12/21	
8		Intel Recommend	0.23	33	Add QT16,QT17,QT18,QT19,QT20 for following Intel DDC	12/21	
9		Intel Recommend	0.3	32	Change UT2 to AT25256B-SSHL-T	12/21	
10	LPC EA FAIL	Fine tune the damping value for EA PASS	0.31	12,28	Change RH267 RH268 RH270 RH271 RH272 to 47ohm for LPC Change R115 R125 R113 R105 R101 to 33ohm for LPC	1/12	
11	Thunderbolt Lanel Fail	Follow INTEL Thunderbolt CRB	0.31	33	Remove RT53 RT57 and RT63 Add DT8	2/2	
12	RF WAKE FAIL at S3	KILL_SWOFF# keep low at S3	0.31	26	Change +3VS_WLAN to +3VALW for SW1	2/2	
13	USB3.0 HDD lost issue S3 resume Fail	U57 USB3.0 Redriver PWR is +3VS	0.31	23	Change U57 PWR to +3V_PCH	2/3	
14	USB3.0 HDD lost issue S3 resume Fail	USB3.0 Redriver PWR is +3VS	0.31	30	Change F10 PWR to +3V_PCH	2/3	
15	RTC timing delay in 40 degree	Change YH1 CAP to samll value	0.31	12	Change CH2 CH3 to 15P	2/3	
16	Pericom USB3.0 Port 2 FAIL	Fine tune Redriver strap setting for Pericom	0.31	23	Add R218 R219 for Pericom USB3.0 Strap	2/3	
17	Thunderbolt Lanel Fail	Intel Recommend	0.32	32	Add RT24,RT43,RT31,RT19 Remove RT21 RT22 CT140 CT141	2/7	
18		ME Design	0.32	31	Change H6 and H32 to 3P_8	2/8	
19		ME Design	0.33	20	Change JCM1 to ACES_50228	2/9	
20		Cysteal EA Report Recommend	0.33	20	Change CT9 CT10 to 12pF	2/9	
21	CRT ripple issue	PCH change stepping, CRT ripple worse than ES2	1.0	17	Change CH36 to 22uF	2/23	
22							
23							
24							
25							
26							

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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses